x86 : Initialization & Devices

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Before the lesson

- Correction & comments about exercises
- Project Presentation
- Context switching in a kernel

x86 power on

- Chips self initialize
- Cpu initialization
- Firmware starting
  - remap itself in memory
  - perform sanity checks (POST)
  - iterate through devices for initialization
  - launch boot code
- Boot code launch OS

BIOS

- 16-bit code
- old, ancient way
- boot MBR partitions (0x55aa)
- user-api is interrupts

BIOS Interrupts

- int $0x10 : Video Services
- int $0x11 : Equipment list
- int $0x12 : lowmem size
- int $0x13 : Disk Services
- int $0x14 : Serial port Services
- int $0x15 : Misc services (0xe820, ...)
- ...

EFI

- 32 or 64 bit code
- New “modern” way
- New partition format
- Interface based api

Example

```
#include <efi.h>

EFI_STATUS main(EFI_HANDLE ImageHandle,
                EFI_SYSTEM_TABLE *SystemTable)
{
  SystemTable->ConOut->Outputstring(
    SystemTable->ConOut, L”Hello World\r\n”);
  return EFI_SUCCESS;
}
```

Different types of Applications

- Applications
- Boot services
- Runtime services
- Drivers

Booting linux

- Linux can boot from multiple modes
  - 16bit
  - 32bit
  - 64bit
  - efi (32 or 64)
- `struct boot_params`

Devices

- Registers accessible to CPU :
  - MMIO
  - PIO (in, out)
- Access to Memory (DMA)
- Interrupts (irq, msi)

Serial Port

- 8250 compatible (or 16550)
- base port on `0x3f8` (for COM1)
- IRQ 4
- ports mapped onto 8250 registers

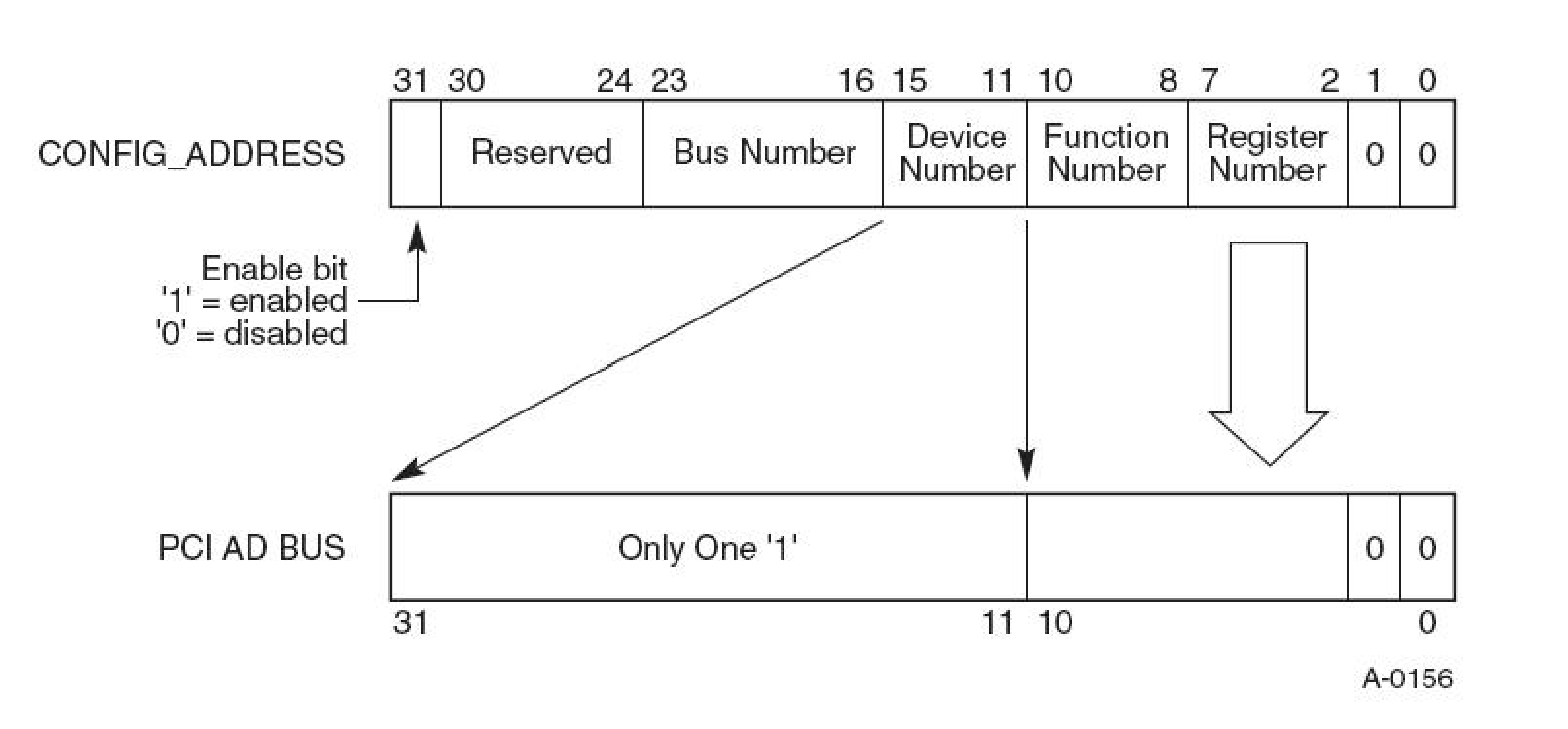
What devices are available ?

- We need some way to discover devices
- When devices are on a bus there is (usually) a way to have their description

PCI Bus

- Configuration space accessed through IO Ports
- `CONFIG_ADDRESS (0xcf8)`
- `CONFIG_DATA (0xcfc)`

PCI Address Structure



PCI Header

31	16	15	0	
Device ID		Vendor ID		00h
Status		Command		04h
Class Code			Revision ID	08h
BIST	Header Type	Lat. Timer	Cache Line S.	0Ch
Base Address Registers				10h
				14h
				18h
				1Ch
				20h
				24h
Cardbus CIS Pointer				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Expansion ROM Base Address				30h
Reserved			Cap. Pointer	34h
Reserved				38h
Max Lat.	Min Gnt.	Interrupt Pin	Interrupt Line	3Ch

ACPI