Introducing the LSE-PC

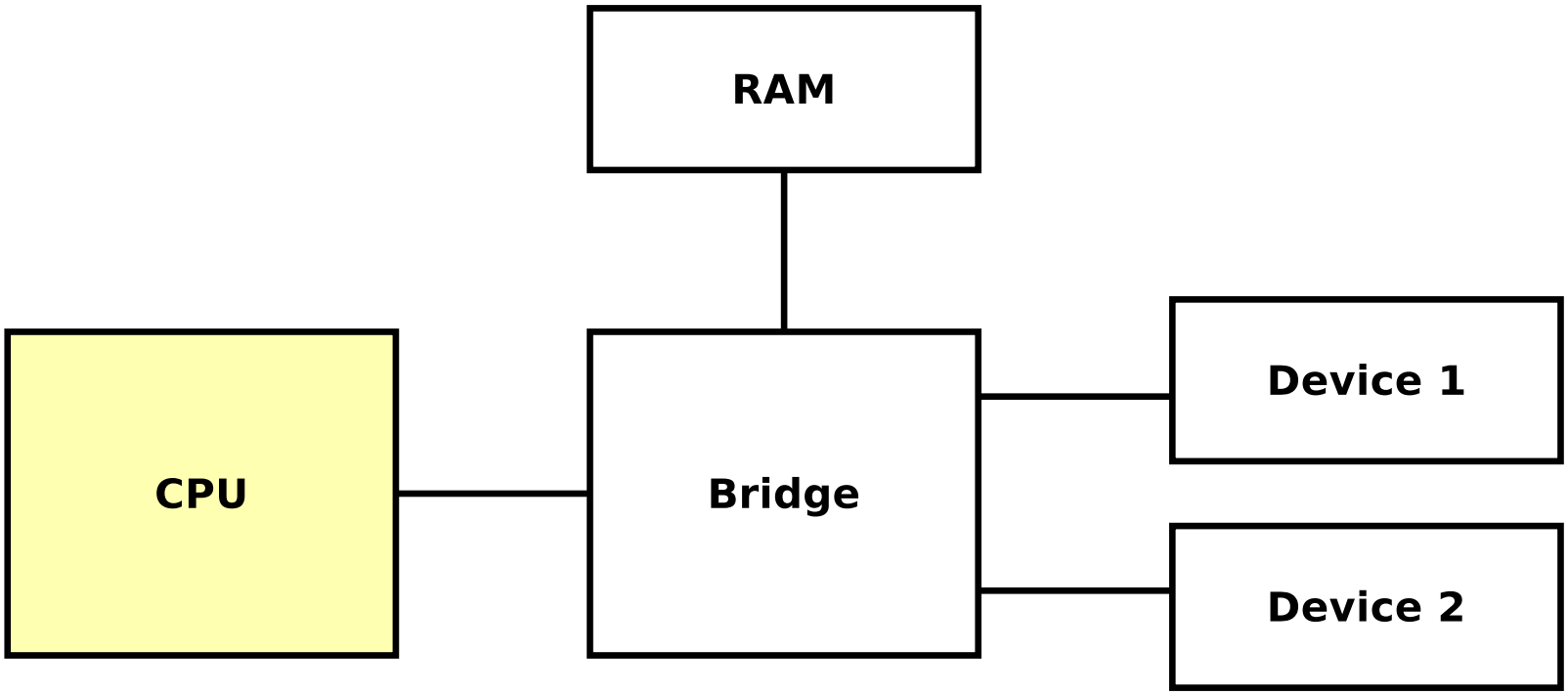
LSE Summer Week 2015

Pierre Surply

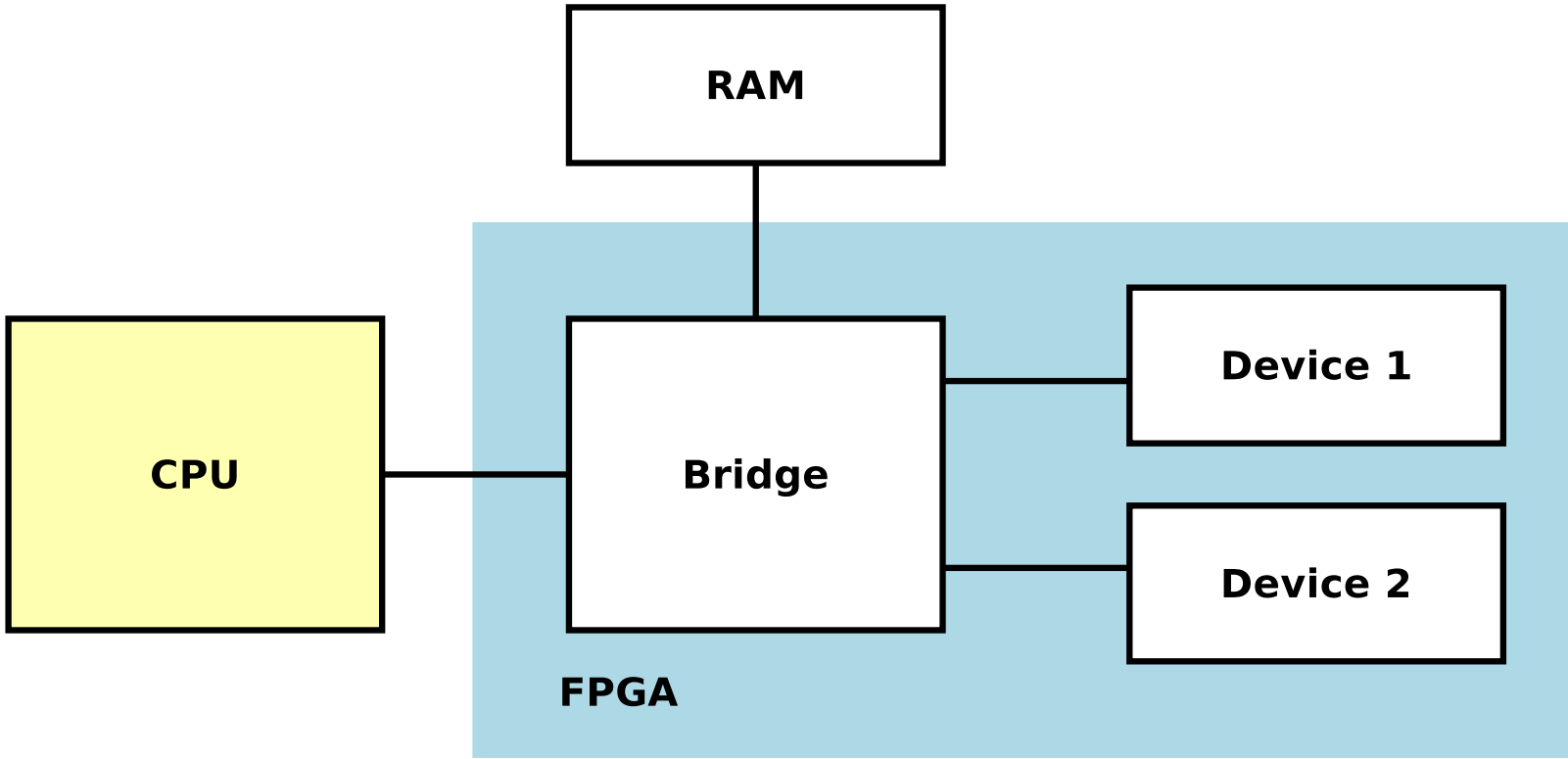
EPITA 2016

July 18, 2015

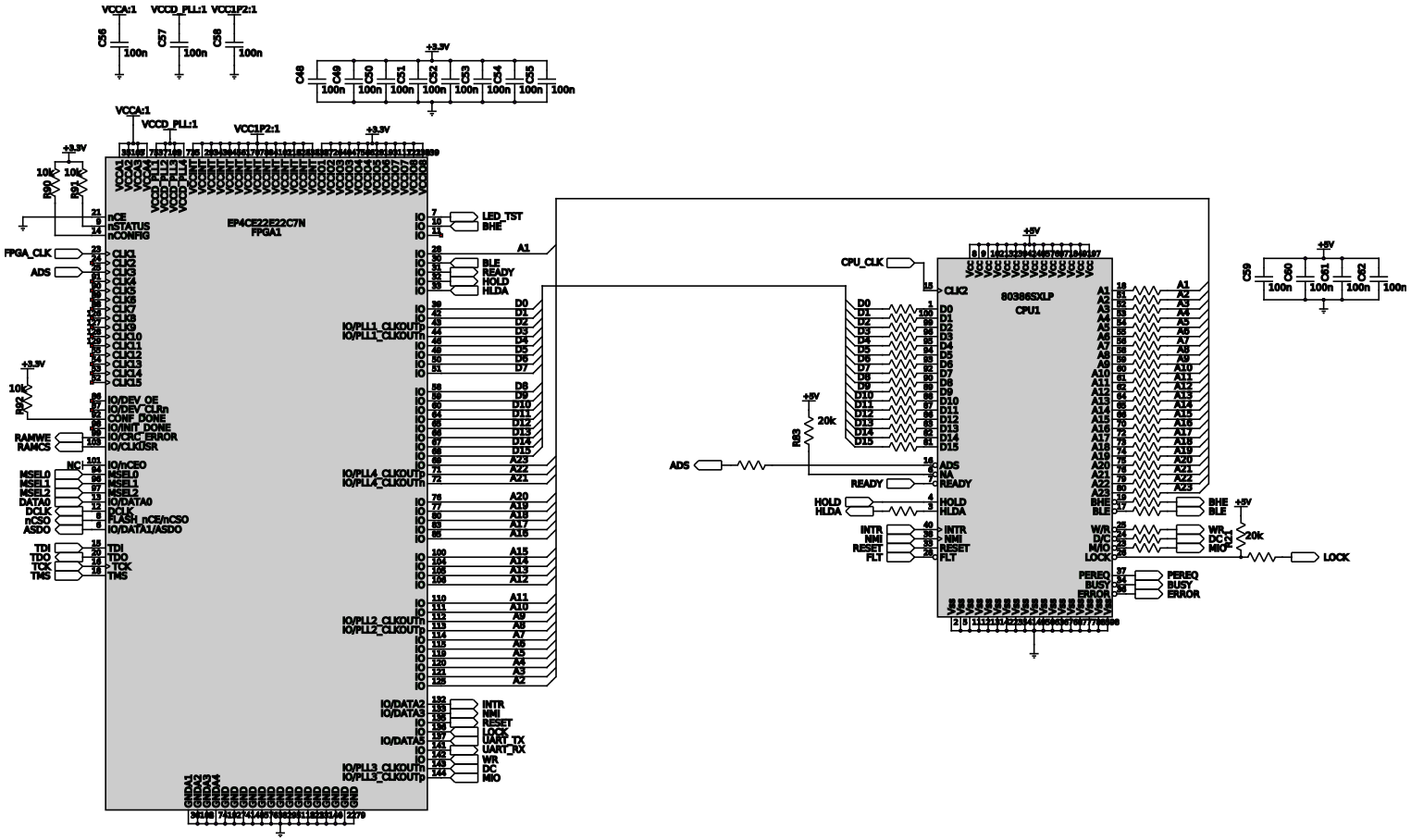
Introduction



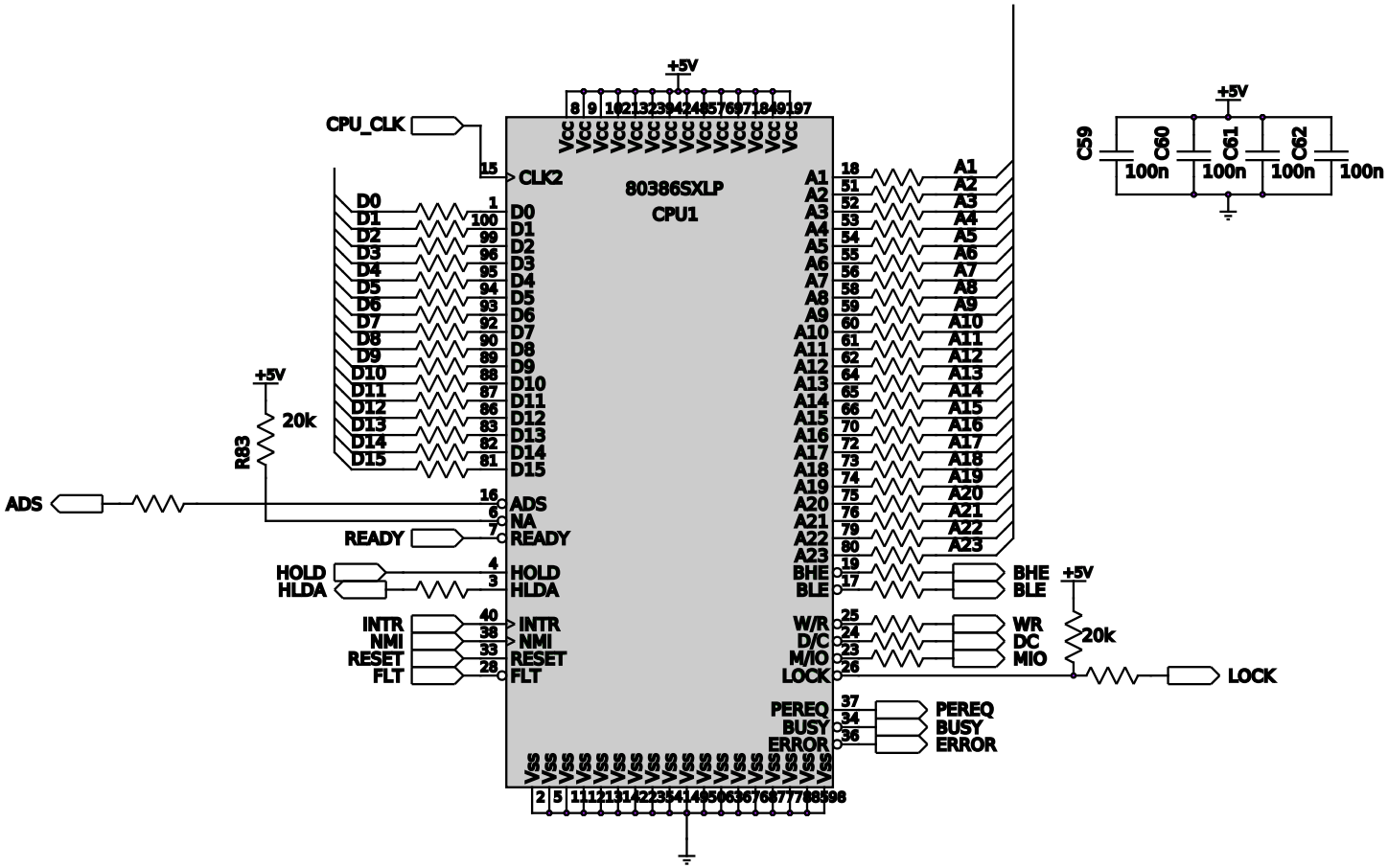
LSE-PC



FPGA - CPU

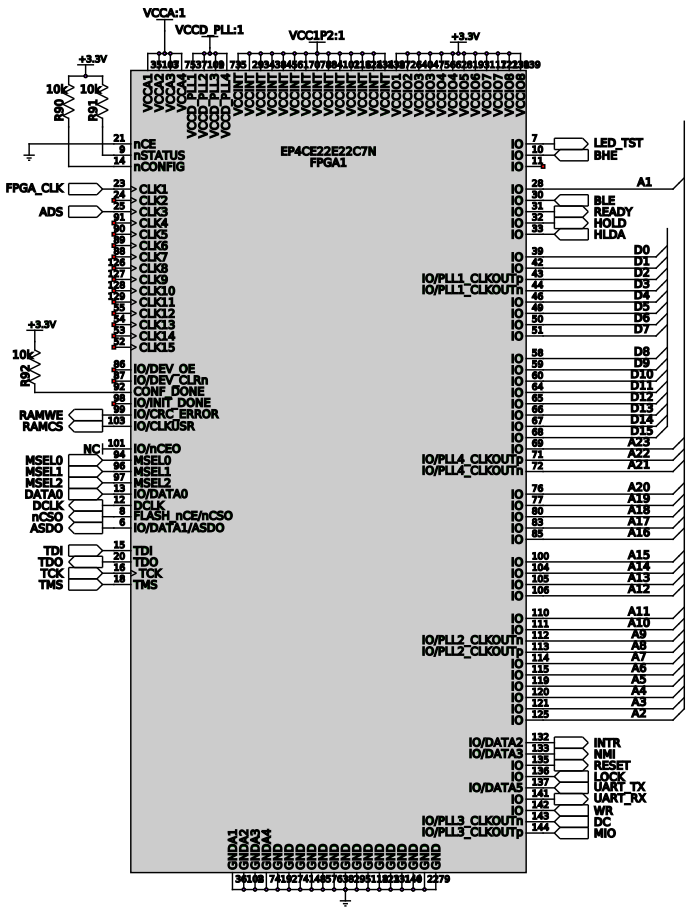


CPU



- NG80386SXLP20: 20MHz 386 SX from 1986

FPGA



- Altera Cyclone IV
- EP4CE22E22C7N
- EQFP 144 pins
- 22320 logic elements
- Released in 2009

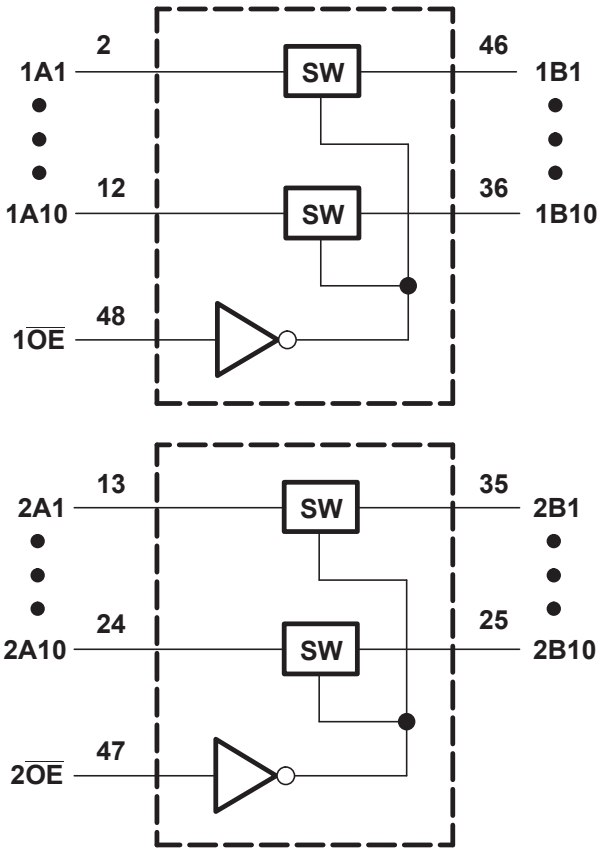
5V Device Compatibility

DGG OR DGV PACKAGE
(TOP VIEW)

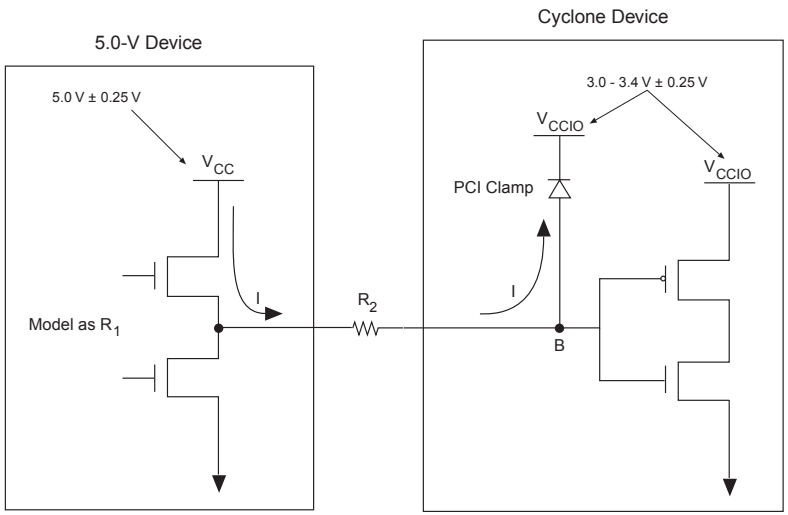
NC	1	48	$1\overline{OE}$
1A1	2	47	$2\overline{OE}$
1A2	3	46	1B1
1A3	4	45	1B2
1A4	5	44	1B3
1A5	6	43	1B4
1A6	7	42	1B5
GND	8	41	GND
1A7	9	40	1B6
1A8	10	39	1B7
1A9	11	38	1B8
1A10	12	37	1B9
2A1	13	36	1B10
2A2	14	35	2B1
V_{CC}	15	34	2B2
2A3	16	33	2B3
GND	17	32	GND
2A4	18	31	2B4
2A5	19	30	2B5
2A6	20	29	2B6
2A7	21	28	2B7
2A8	22	27	2B8
2A9	23	26	2B9
2A10	24	25	2B10

NC - No internal connection

LOGIC DIAGRAM (POSITIVE LOGIC)



5V Device Compatibility



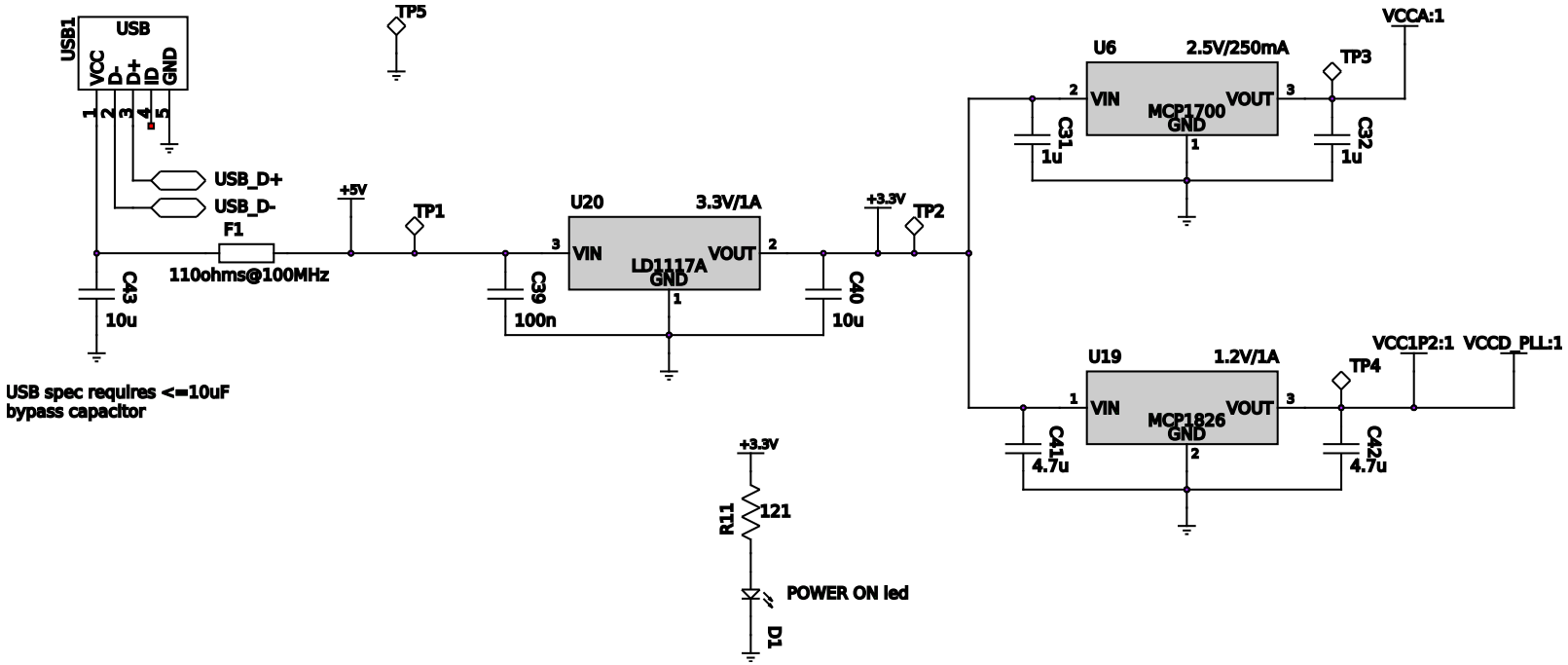
$$R1 = \frac{V_{CC}}{I_{OH}}$$

$$V_{IN} = V_{CCIO} + 0.7V$$

$$R2 = \frac{(V_{CC} - V_{IN}) - (R1 \times I_{OH})}{I_{OH}}$$

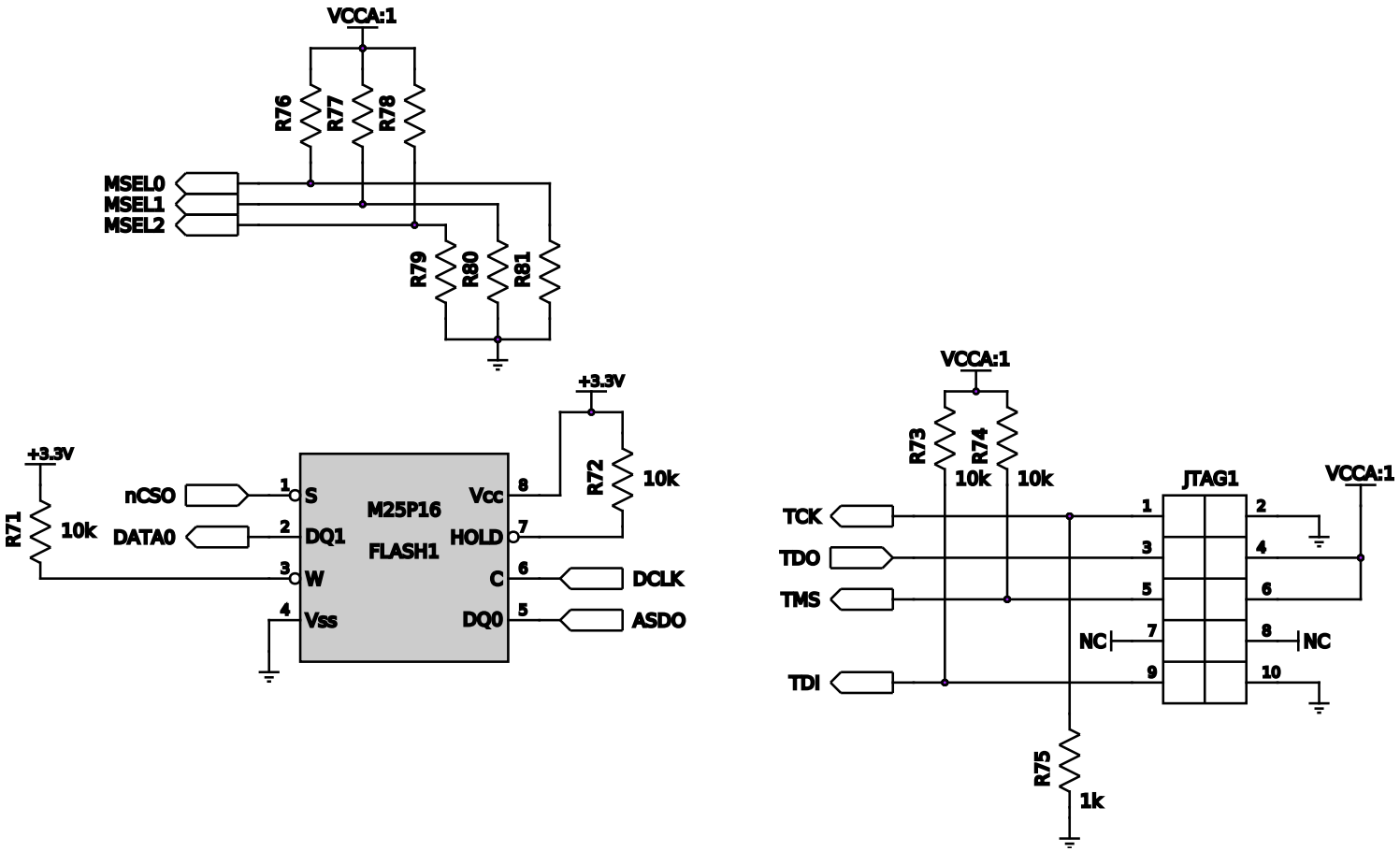
$$R2 = 120\Omega$$

Voltage Regulation



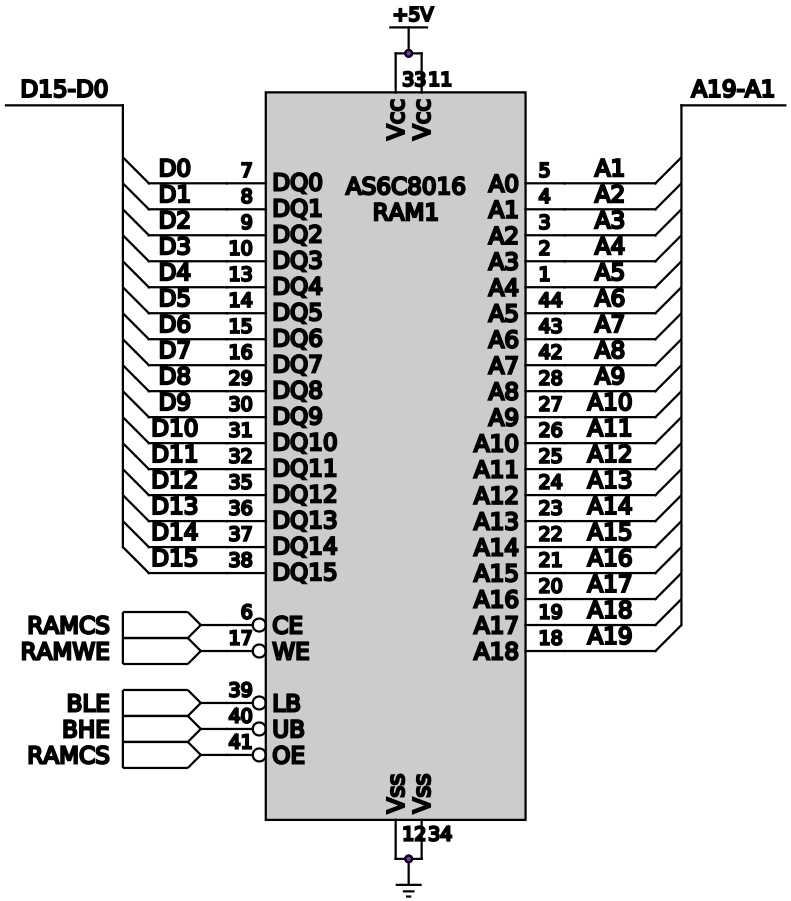
- *5V*: CPU, SRAM
- *3.3V*: FPGA In/Out
- *2.5V*: FPGA Analog PLL
- *1.2V*: FPGA internal logic, Digital PLL

FPGA Configuration



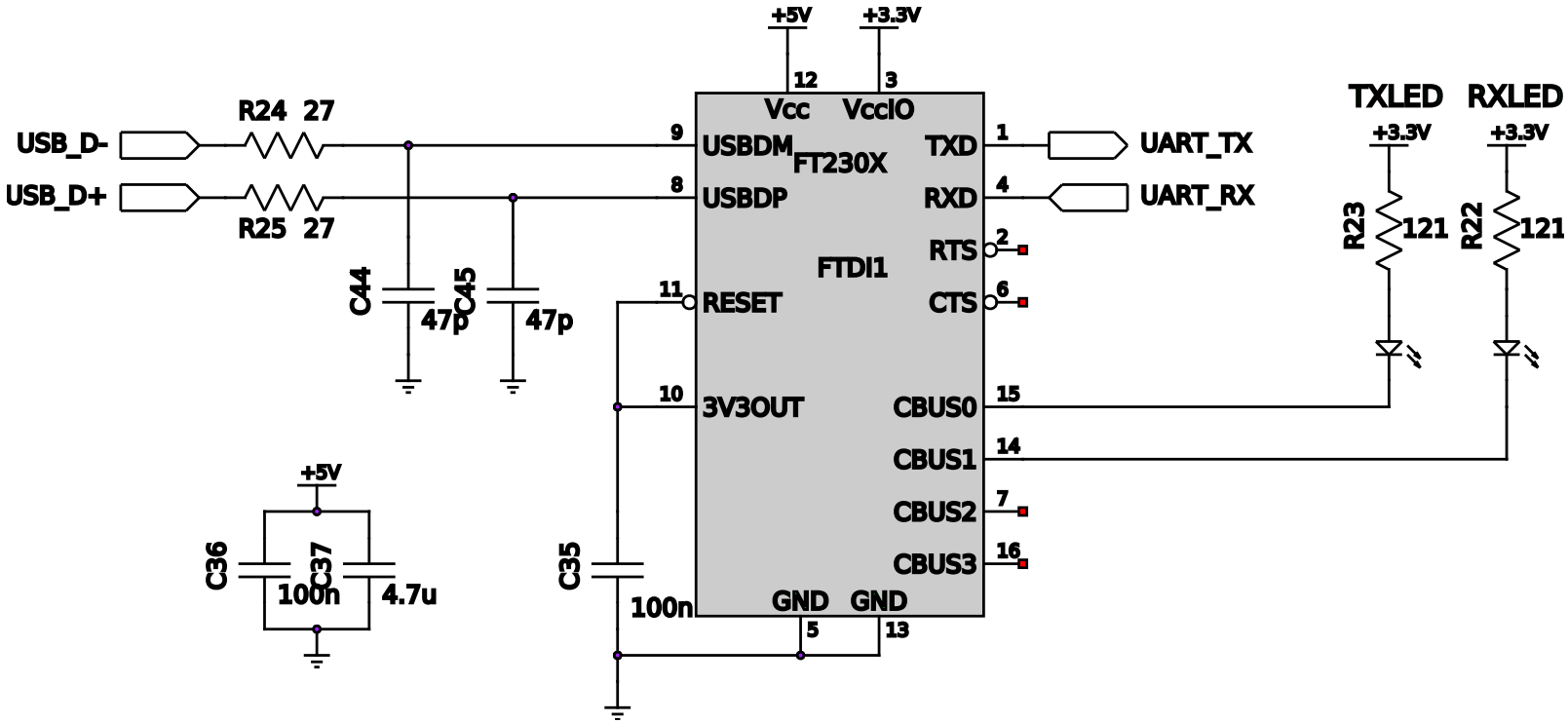
- M25P16: 16Mbits Serial Flash (SPI)
- MSEL: Active Serial Programming

Static RAM



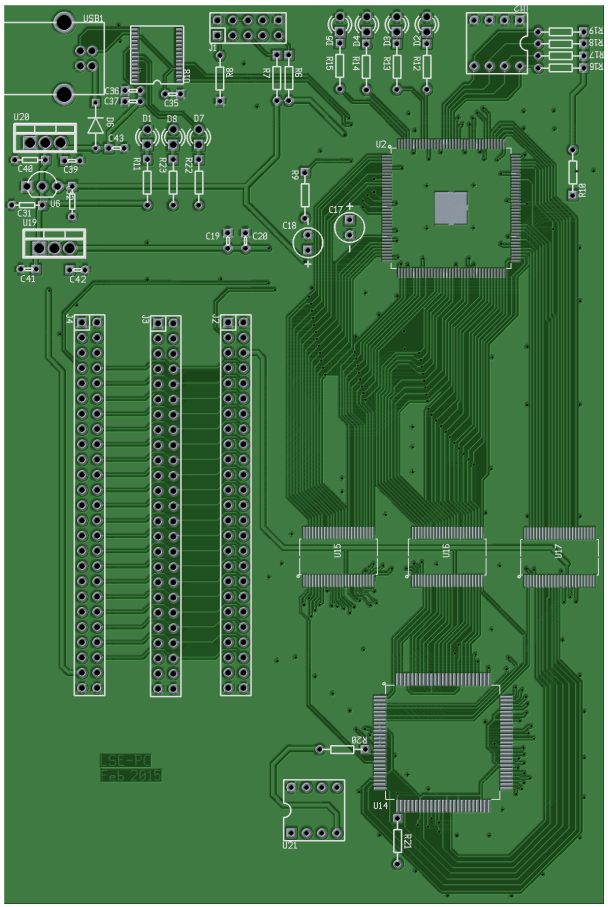
- Alliance Memory
- AS6C8016
- Static RAM
- 512K $\times$ 16bits

USB

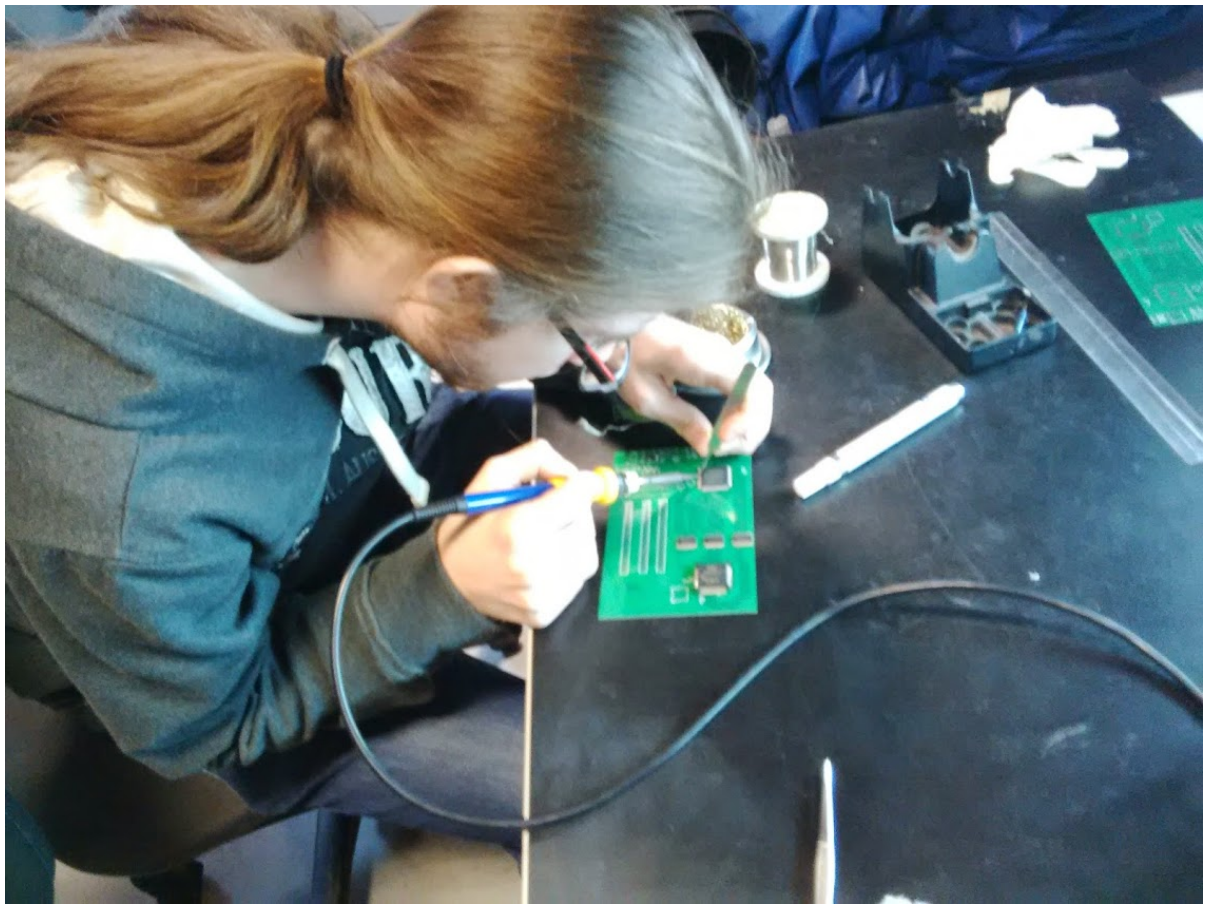


- FT230: USB/UART bridge

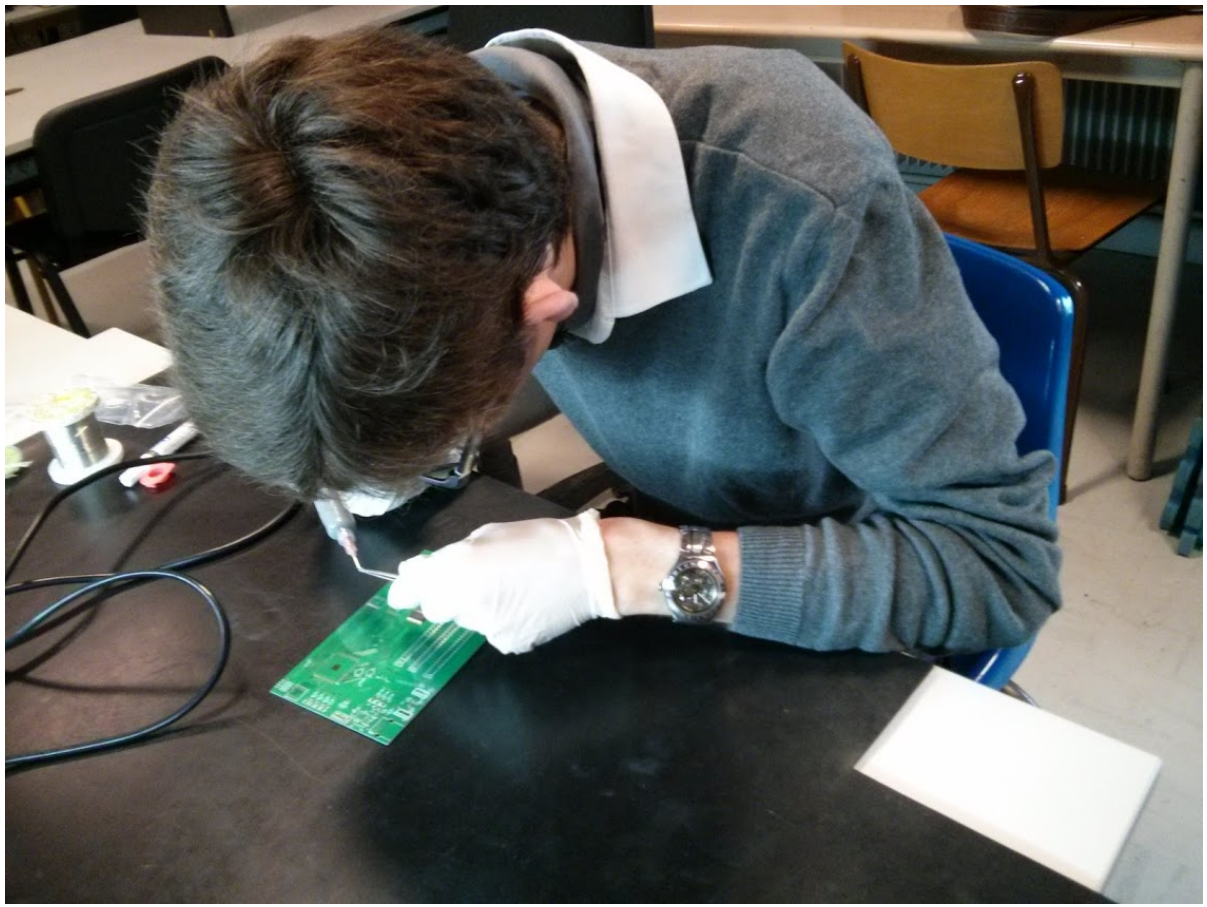
Version 1.0



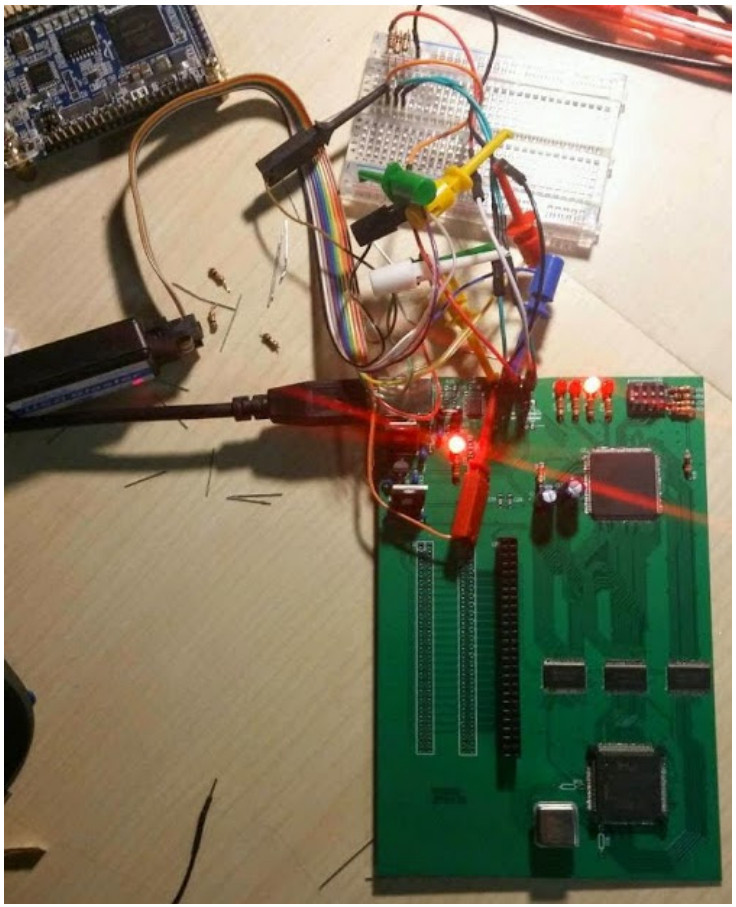
Soldering



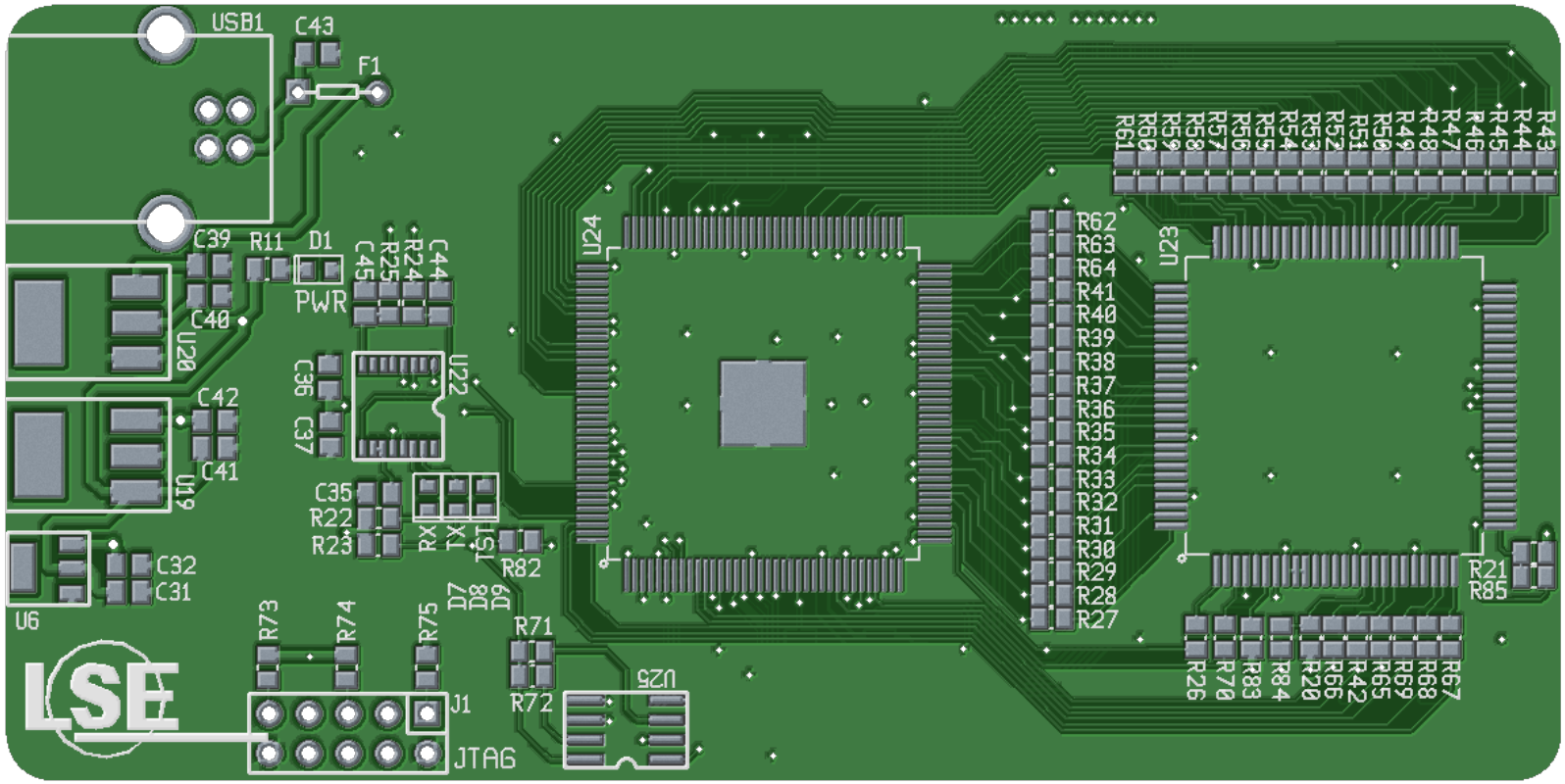
Soldering



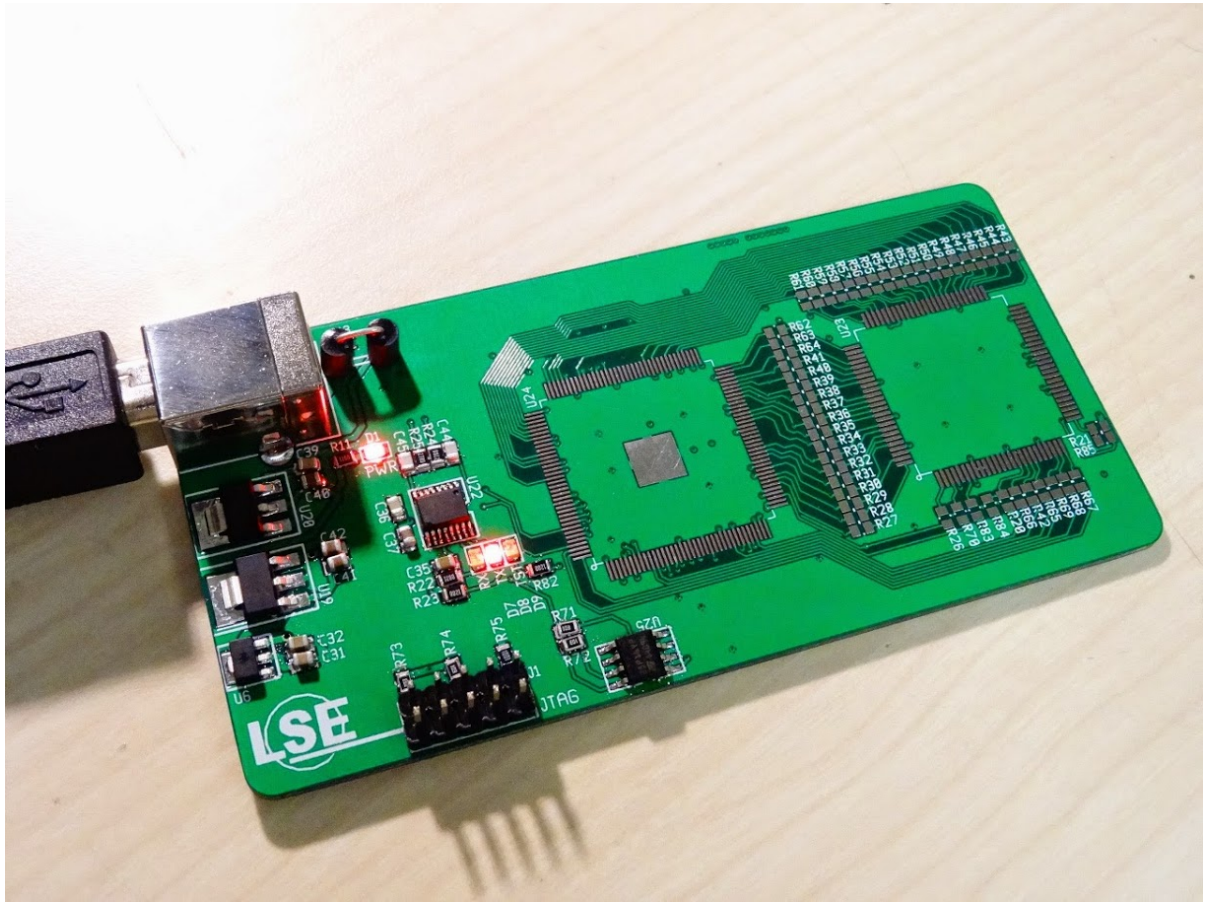
Version 1.1



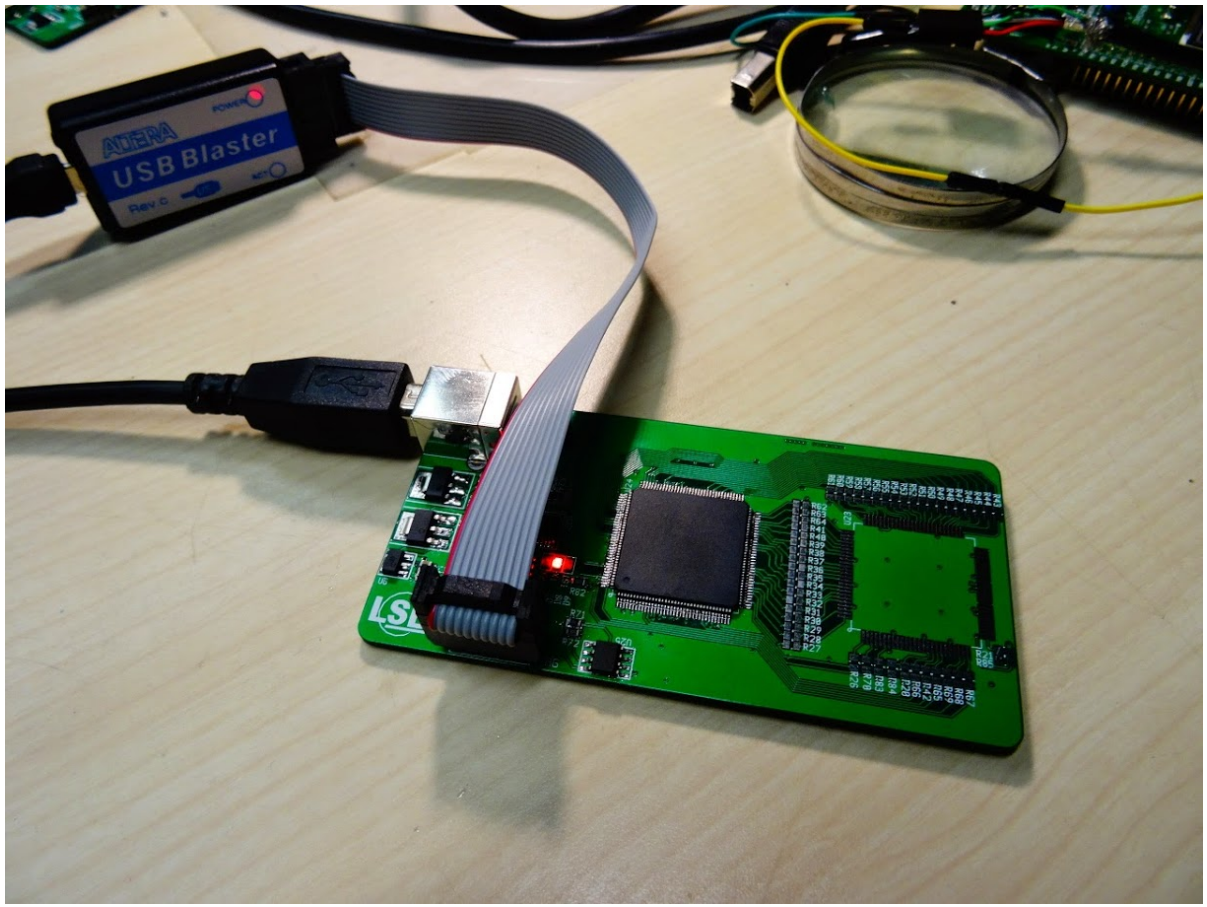
Version 2.0



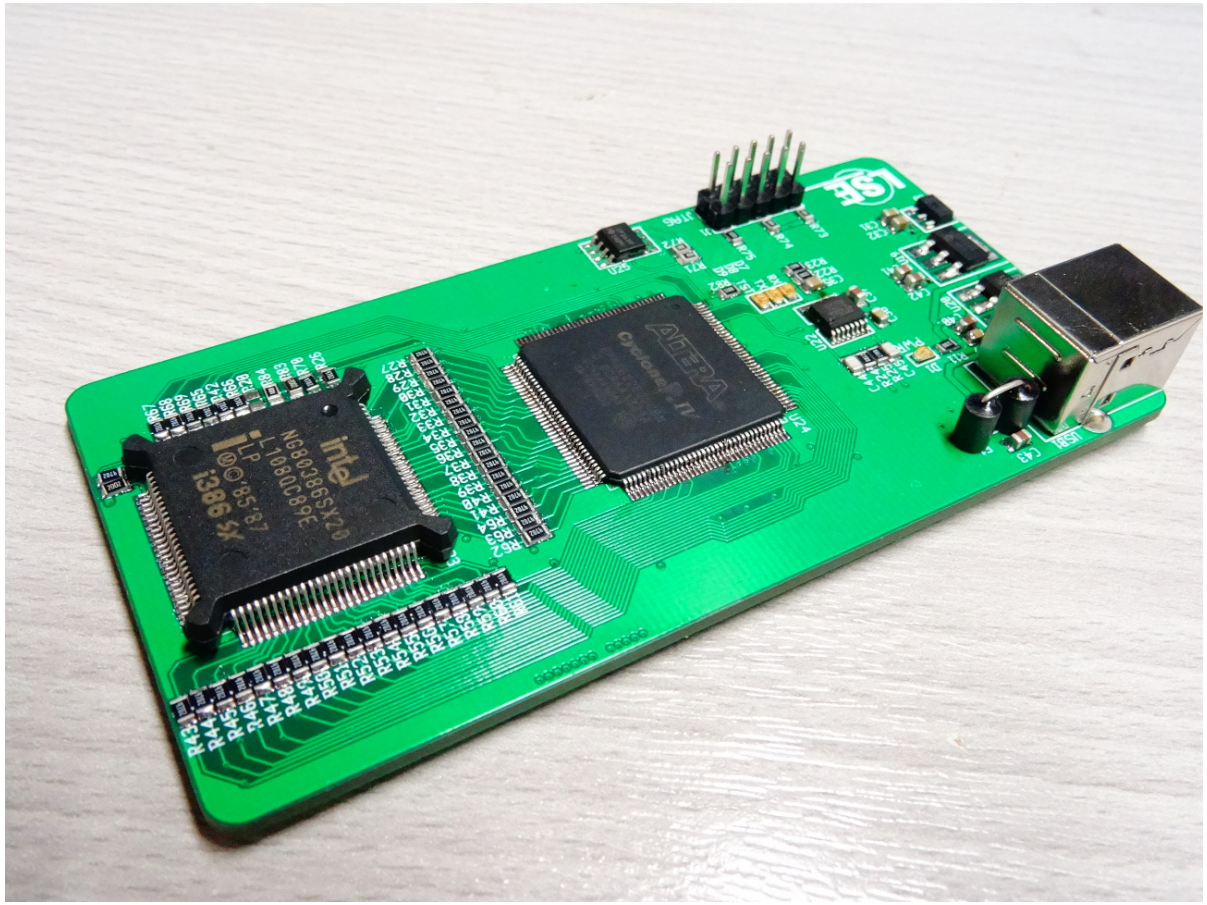
Version 2.0



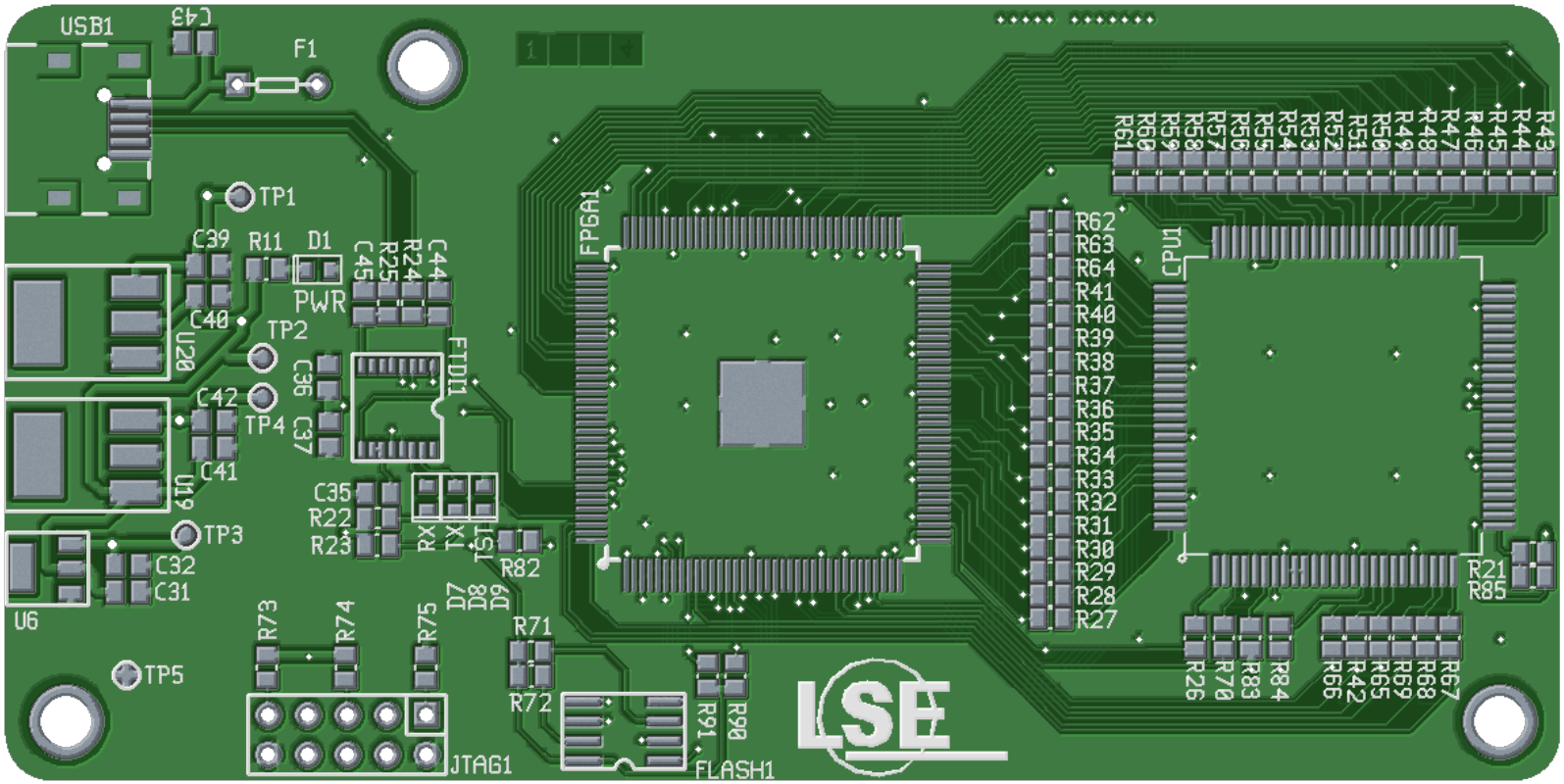
Version 2.0



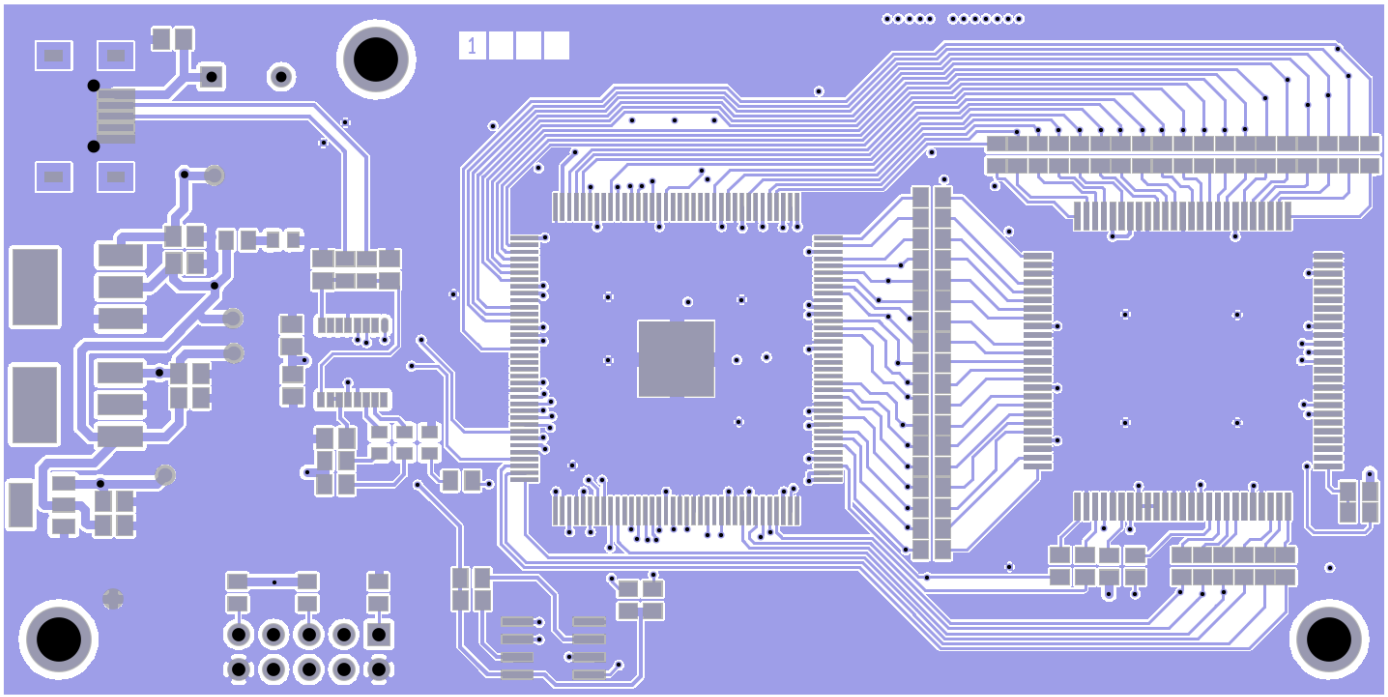
Version 2.0



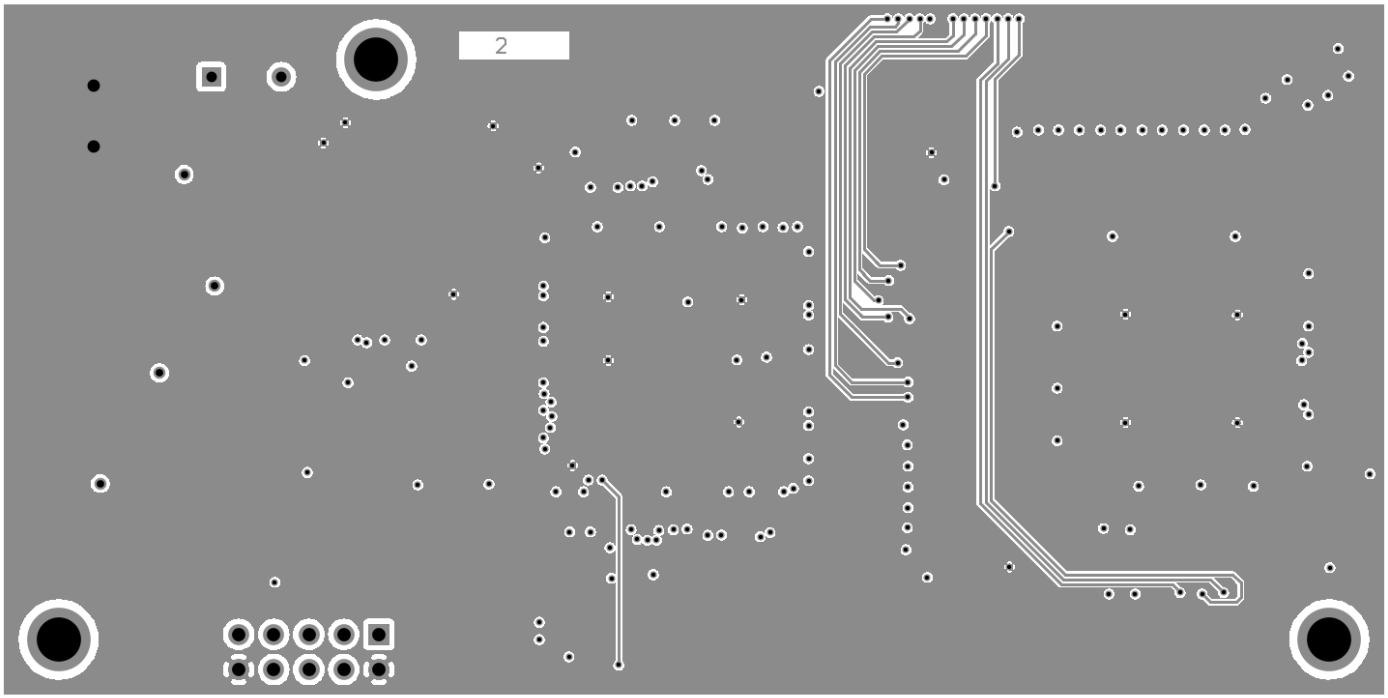
Version 3.0



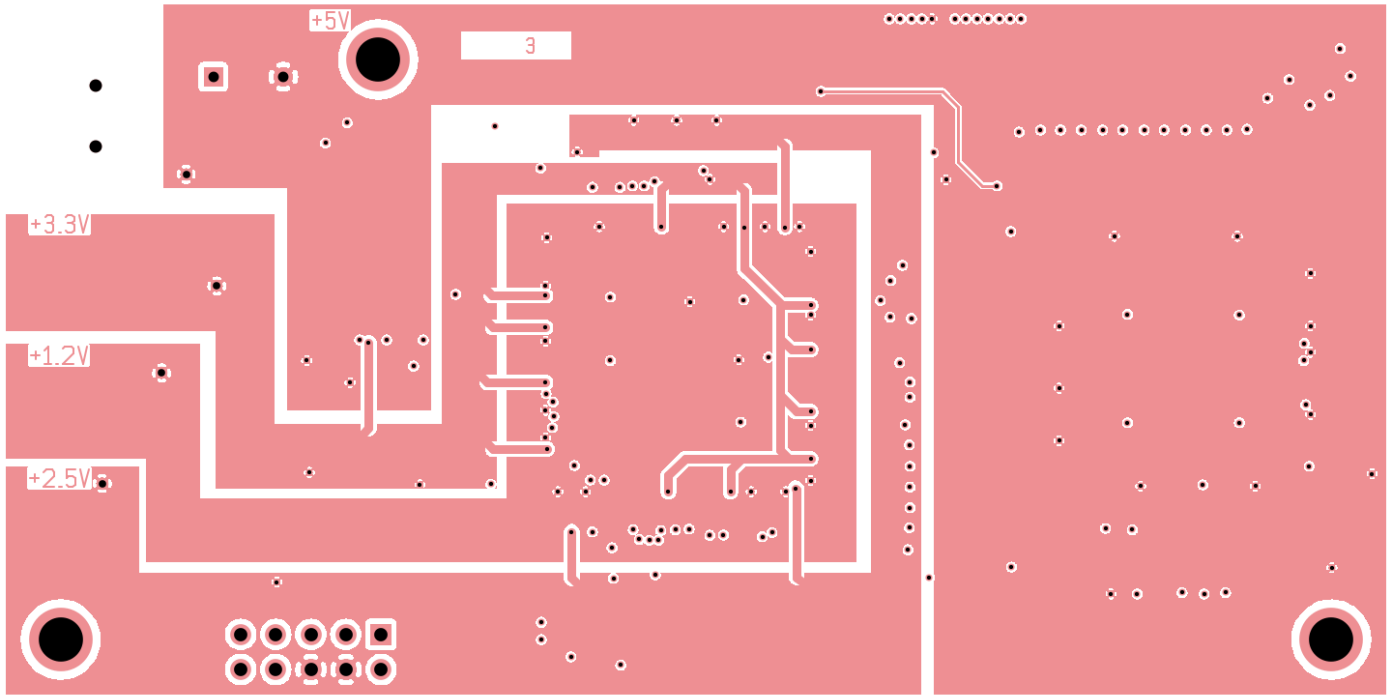
Top Layer



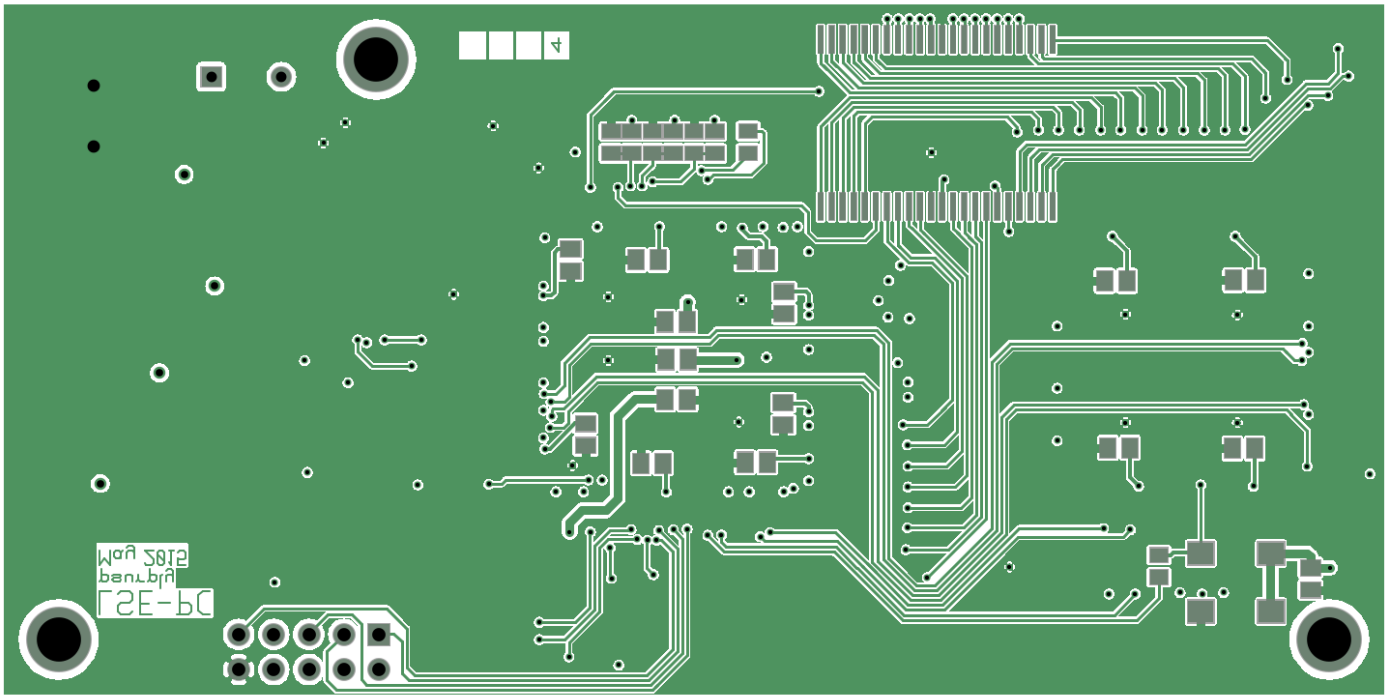
Ground Layer



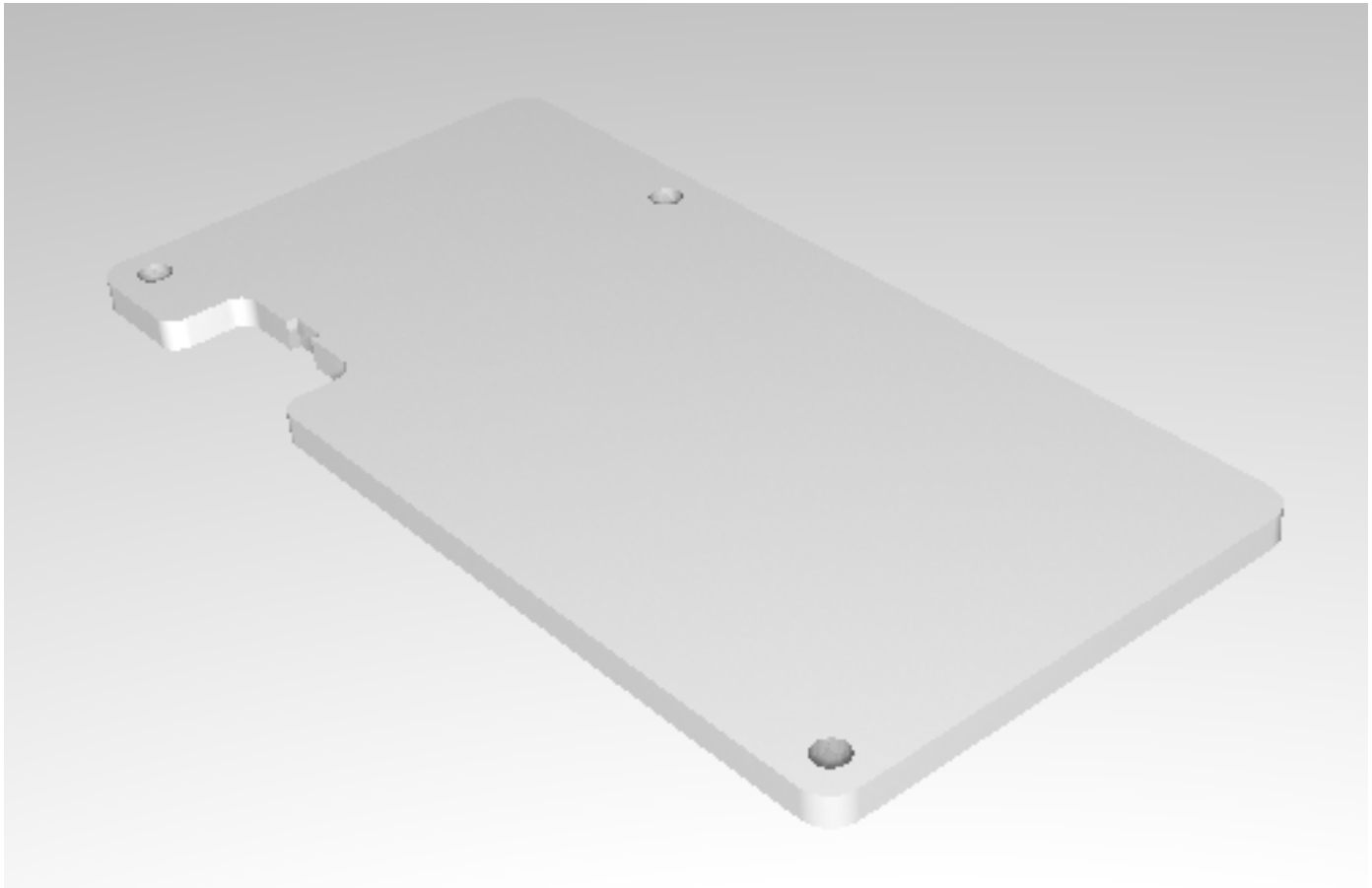
Power Layer



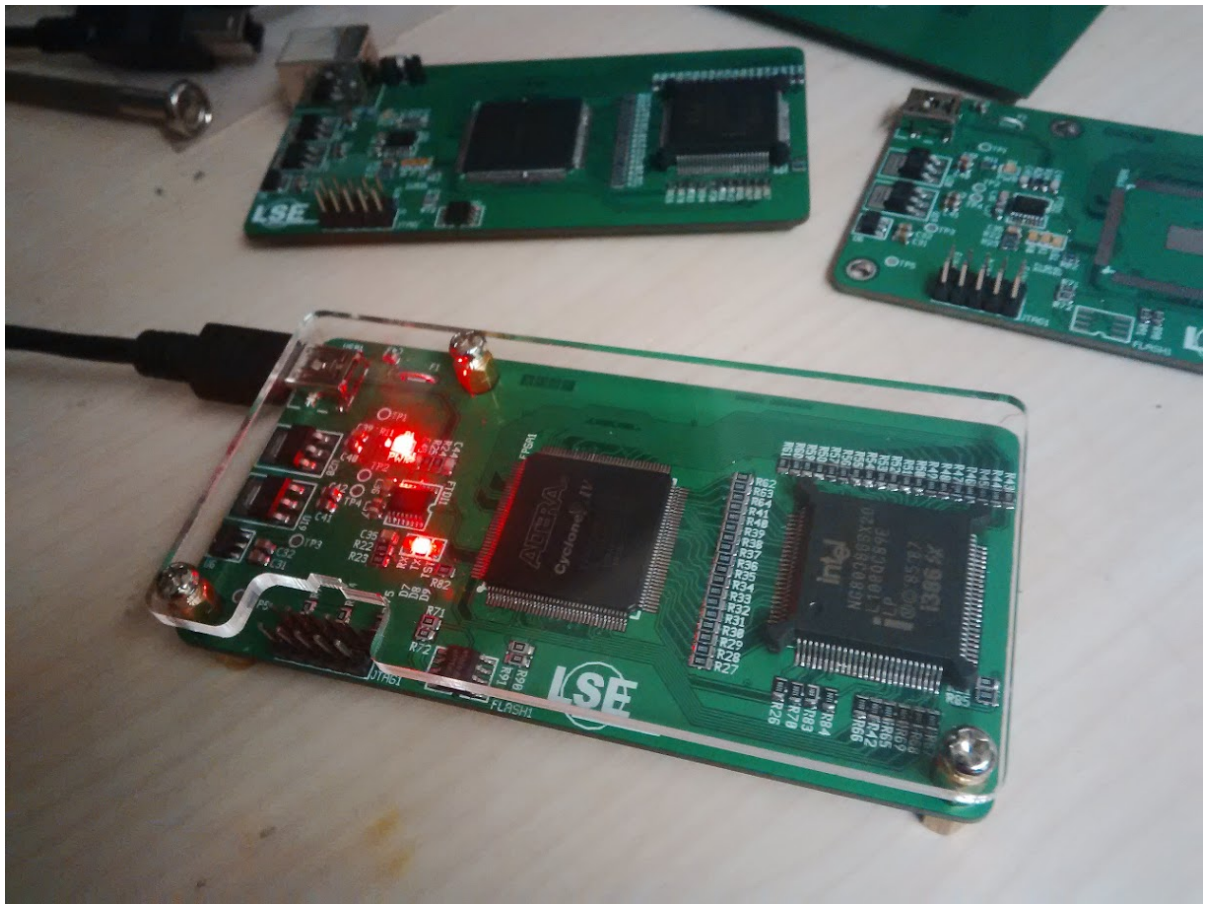
Bottom Layer



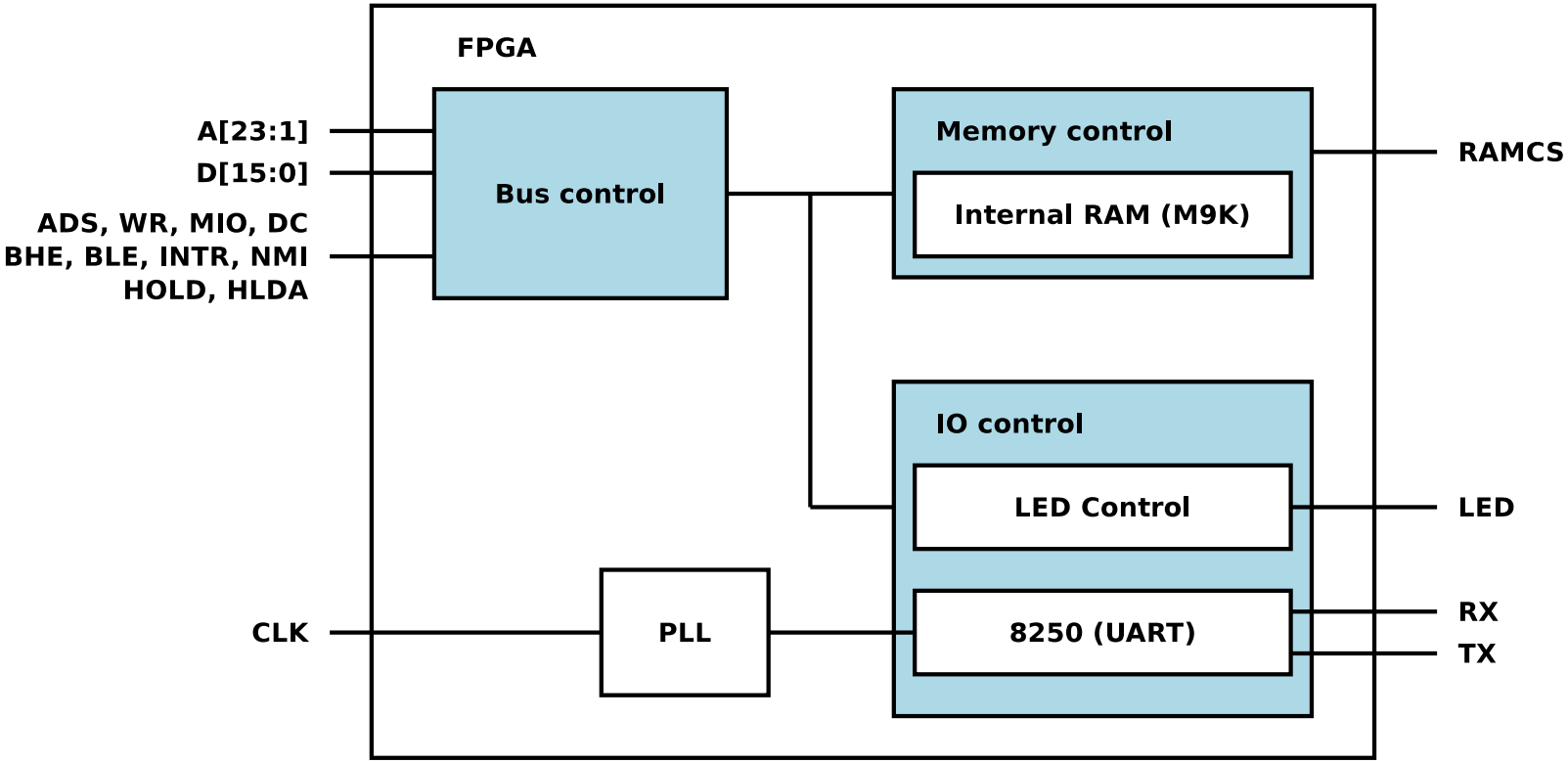
Version 3.0



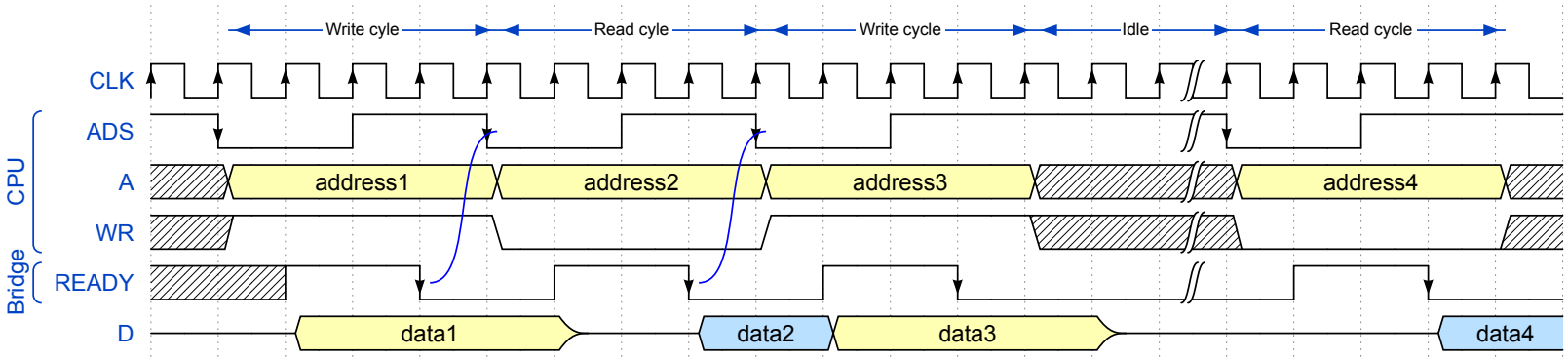
Version 3.0



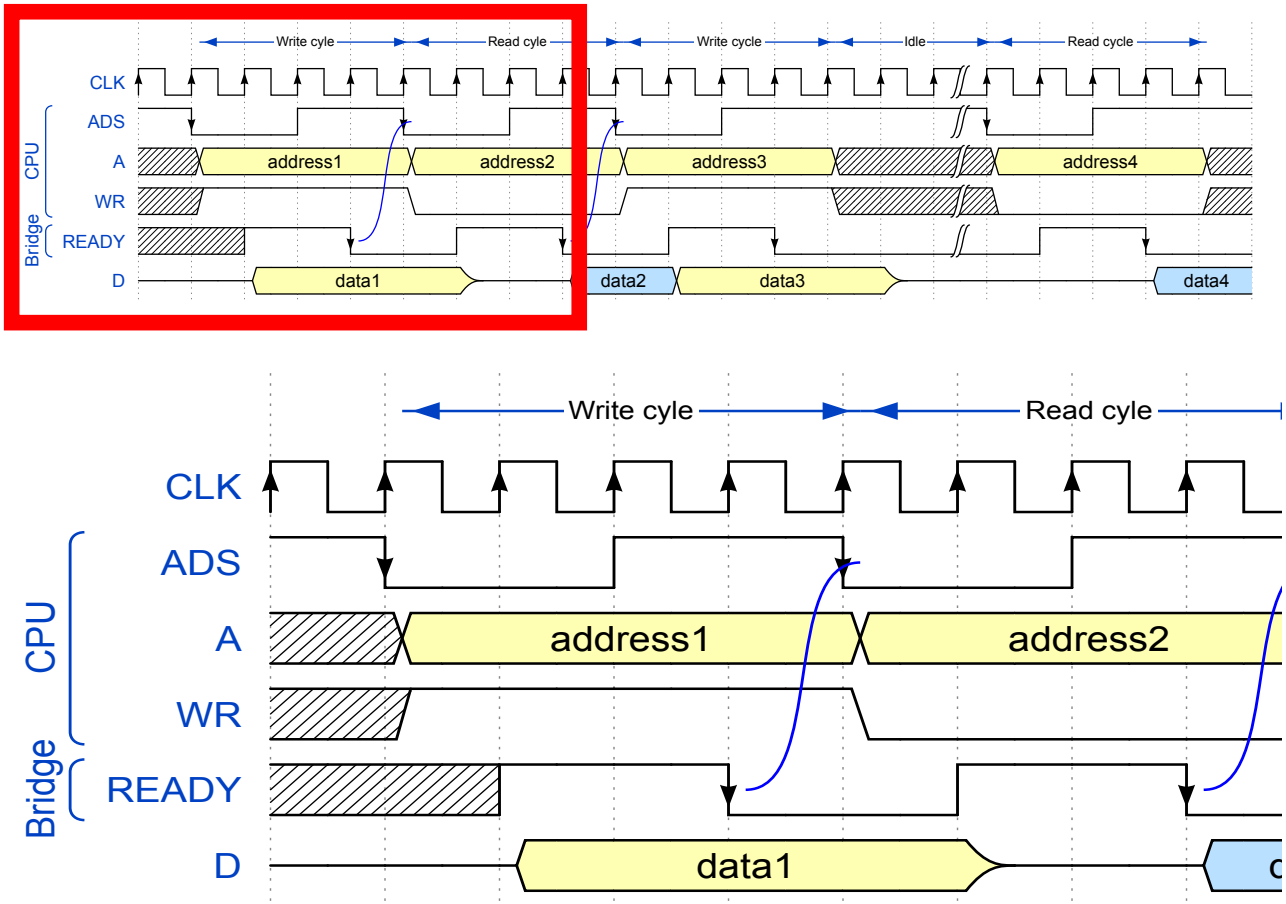
FPGA Design Overview



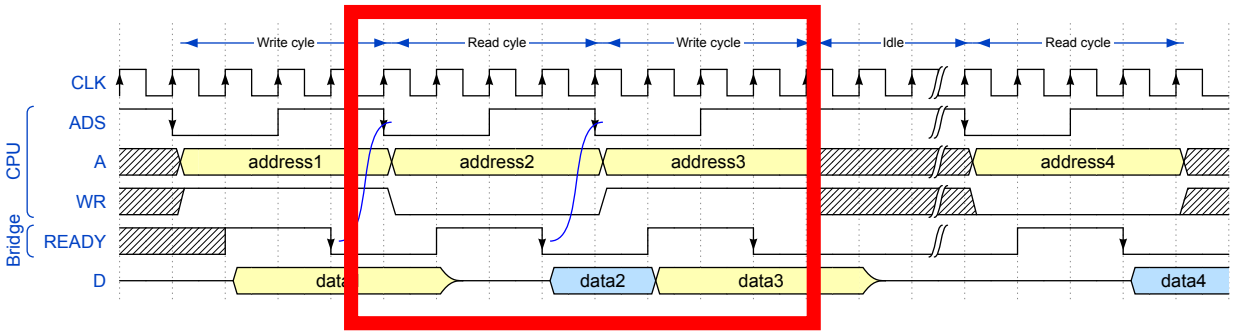
Bus Controller

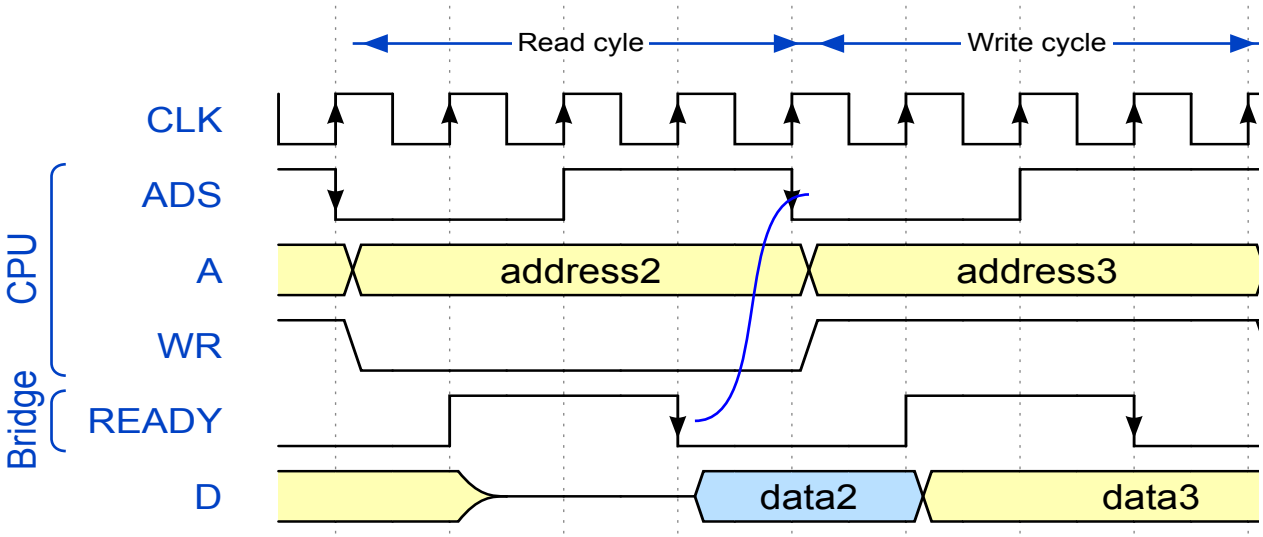


Bus Controller

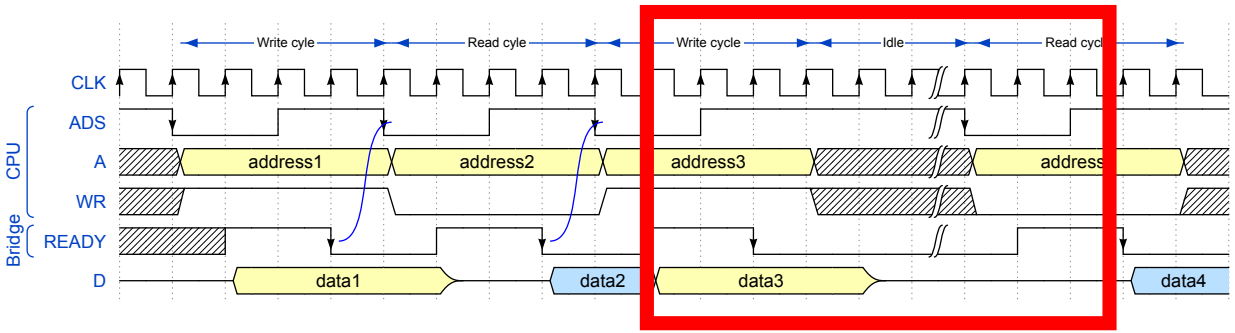


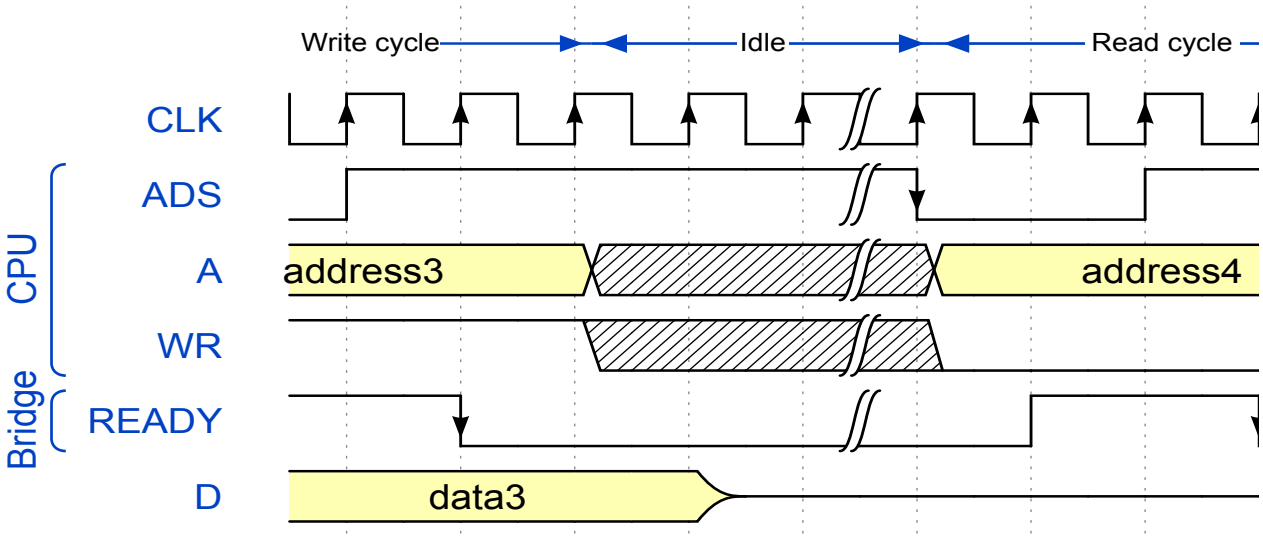
Bus Controller



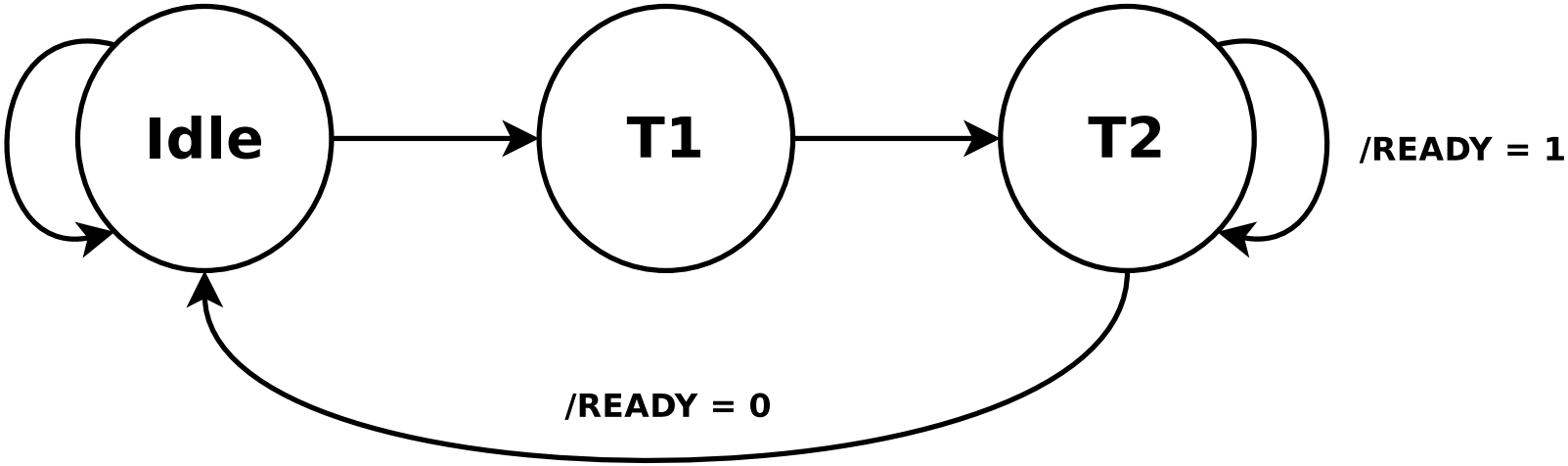


Bus Controller



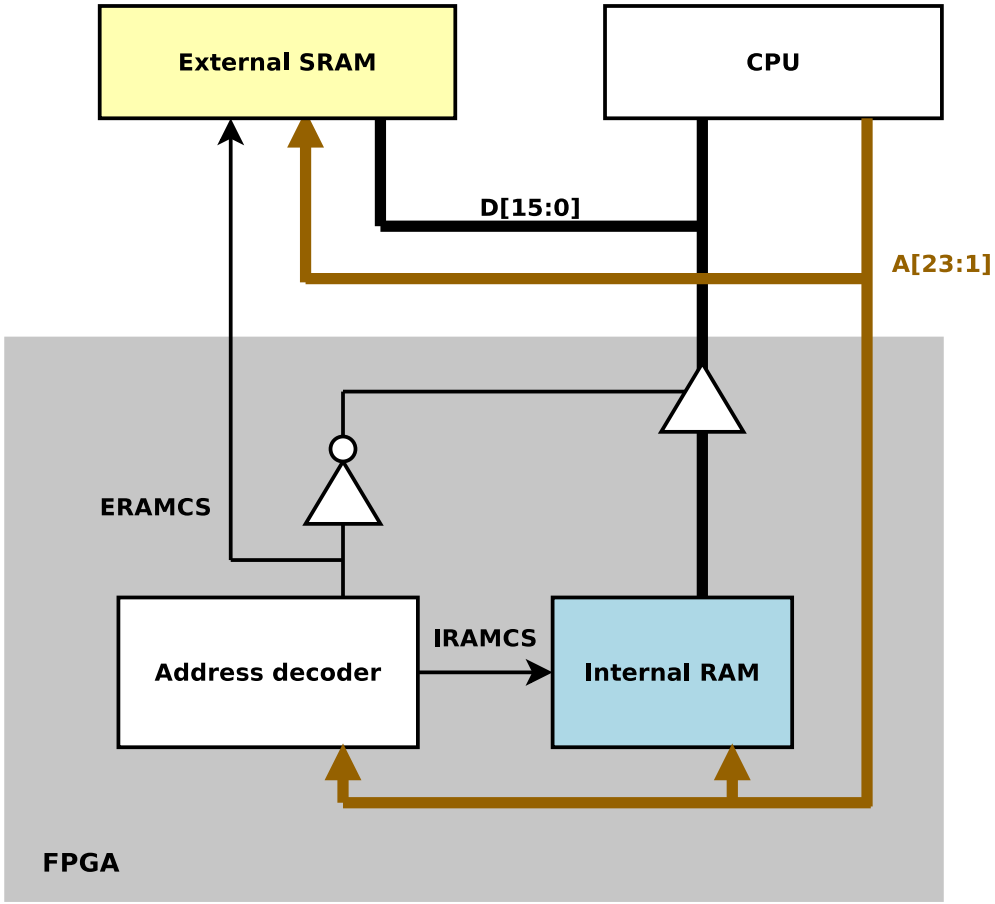


Bus Controller

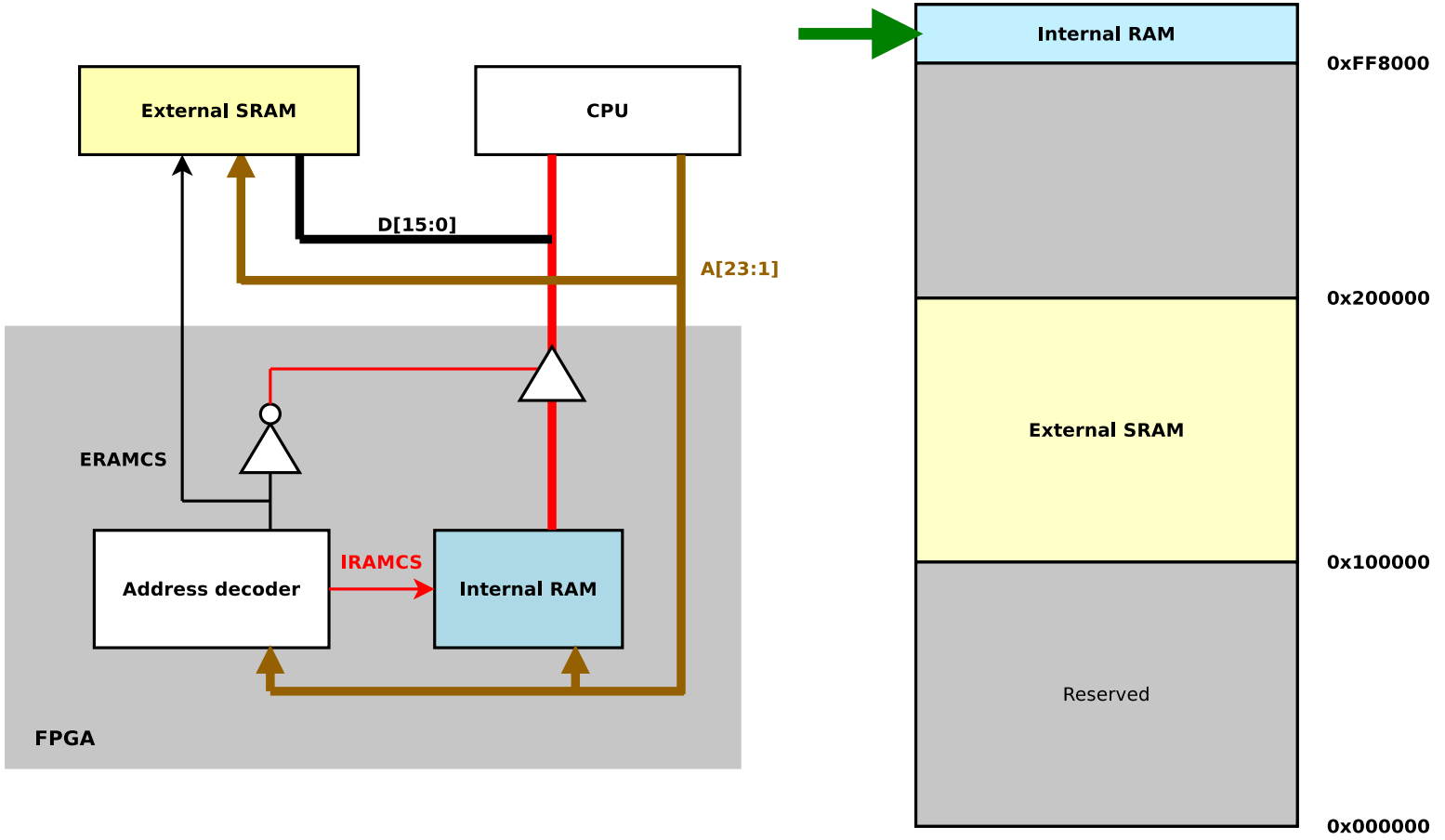


- *T1*:
  - ADS $\leftarrow$ 0
  - A $\leftarrow$ *Requested address*
  - If write cycle, D $\leftarrow$ *Data to write*
- *T2*:
  - ADS $\leftarrow$ 1
  - If read cycle, *Data to read* $\leftarrow$ D

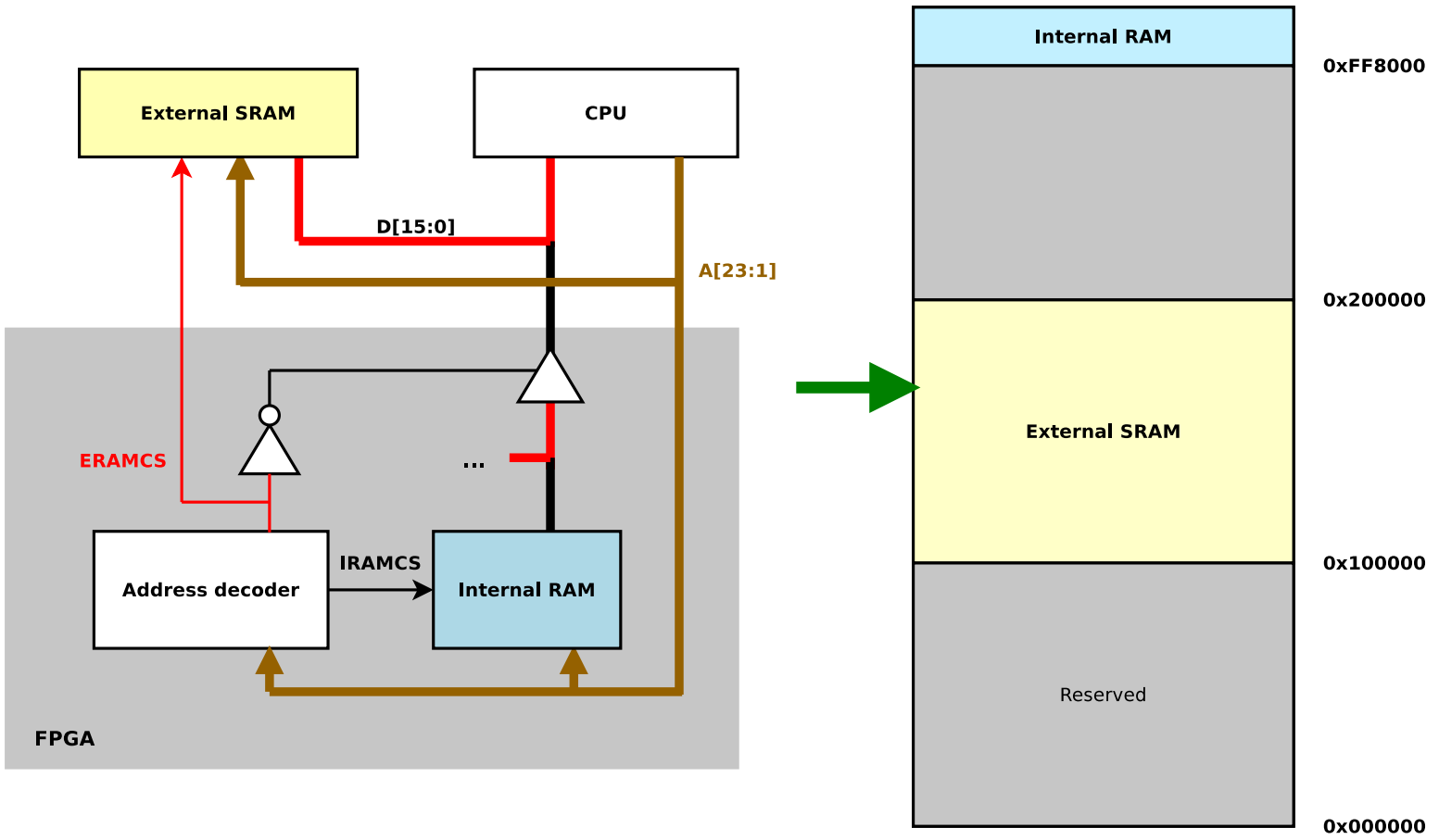
Memory Controller



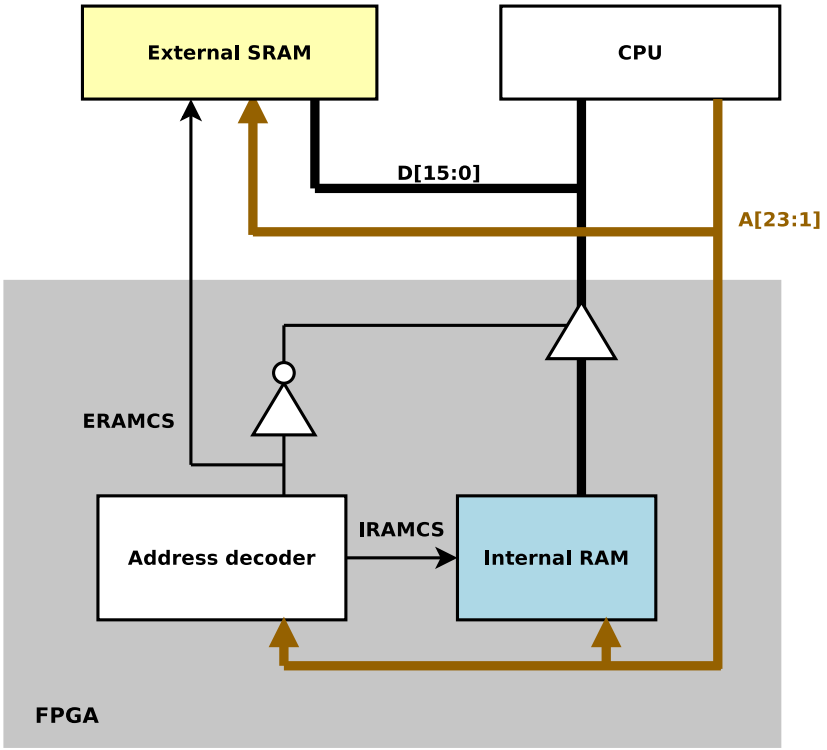
Memory Controller

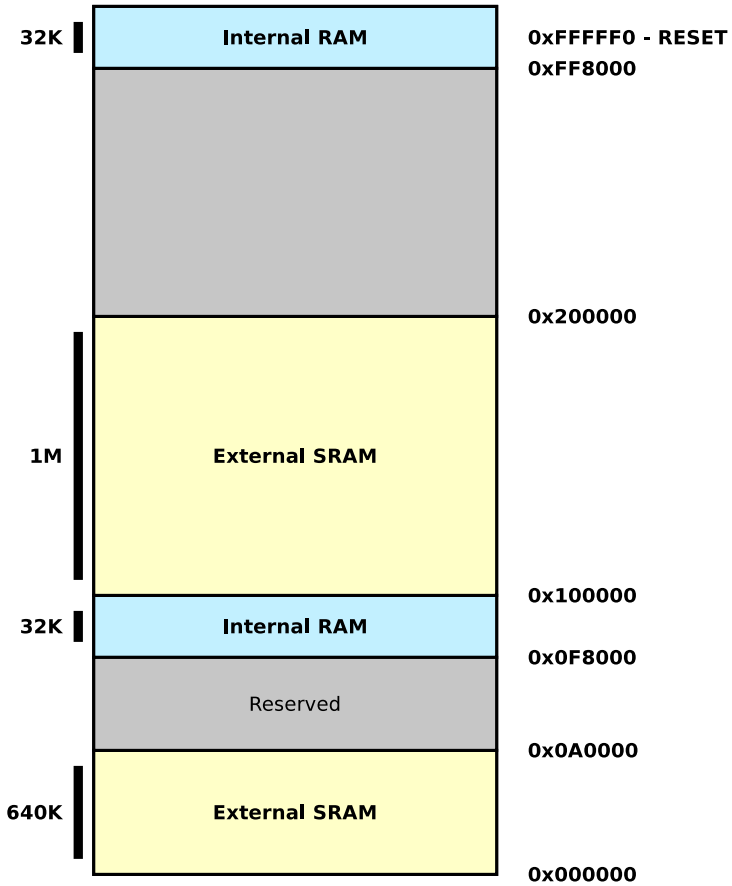


Memory Controller

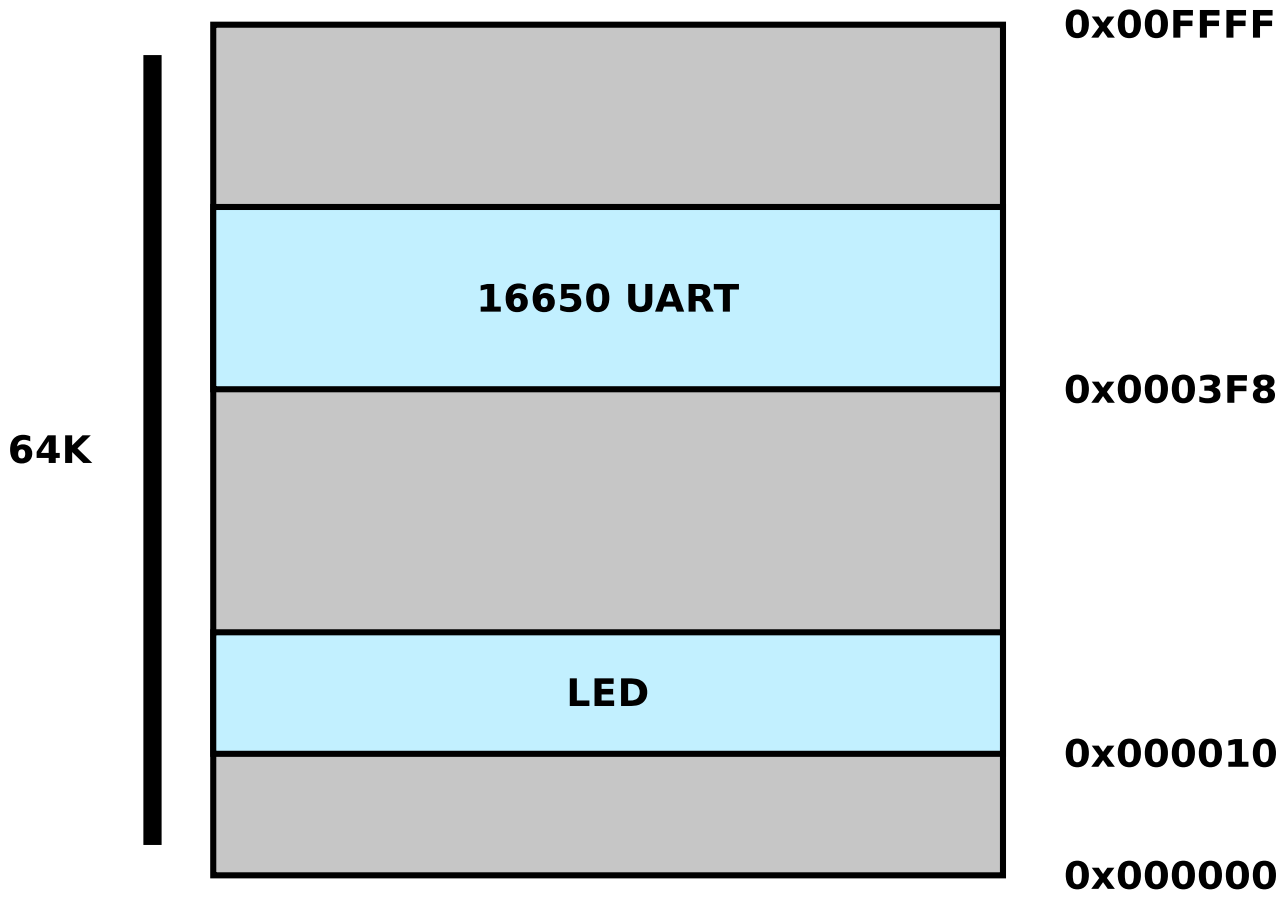


Memory Controller



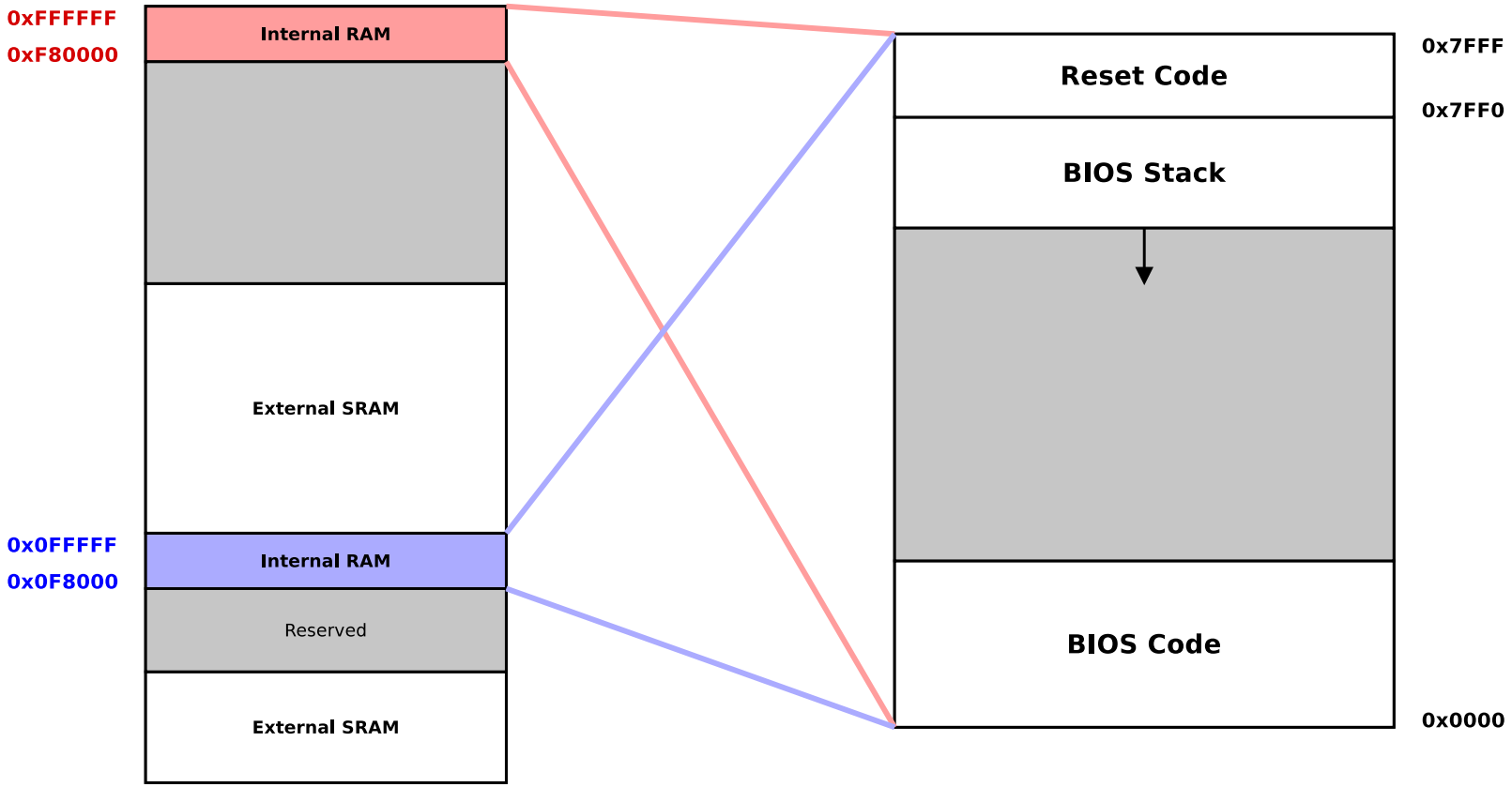


I/O Controller




```
in al, 0x10
xor al, 1
out 0x10, al
```

Internal RAM layout



Reset

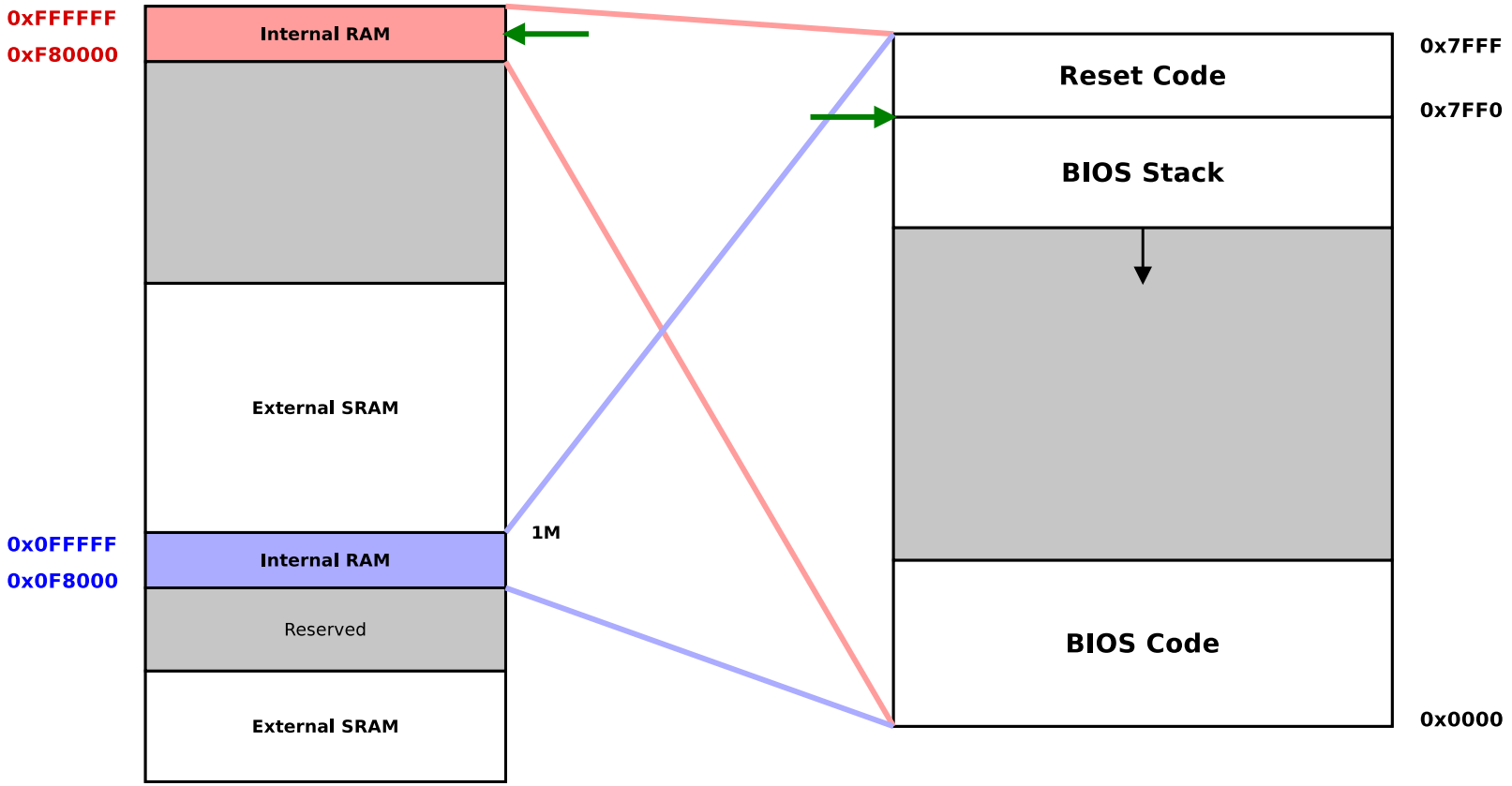

```
org 0xFFF0
reset:
    mov ax, 0xF000
    mov ds, ax
    mov ss, ax
    mov sp, 0xFFF0
    jmp 0xF000:0x8000
```

```
FFFFF0: 00b8 8ef0 8ed8 bcd0 fff0 00ea 0080 00f0
```

Reset address

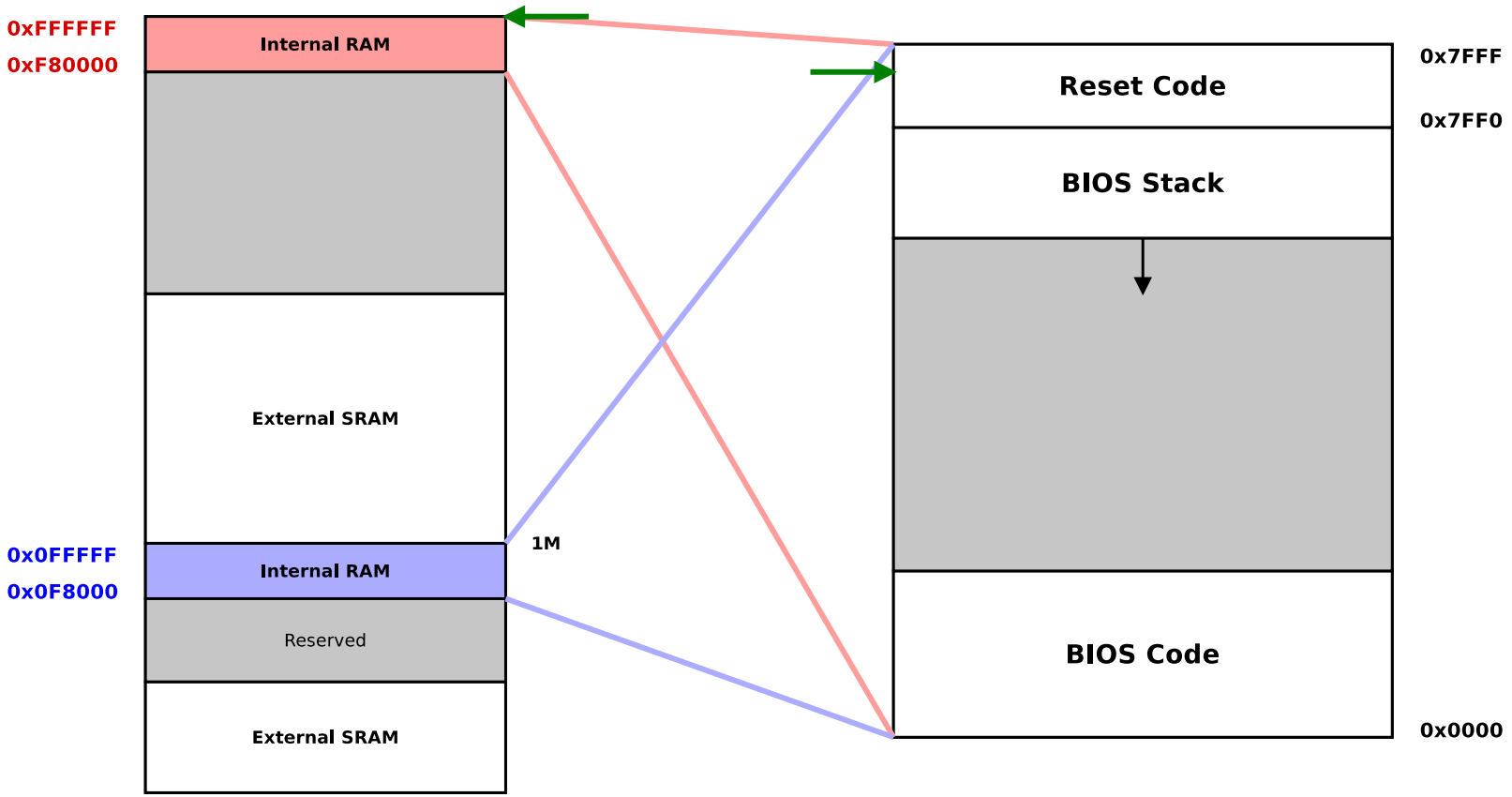
```
            CS:    F000
            IP:  +  FFF0
               ------------
 Reset Address:   FFFFF0
```

Reset



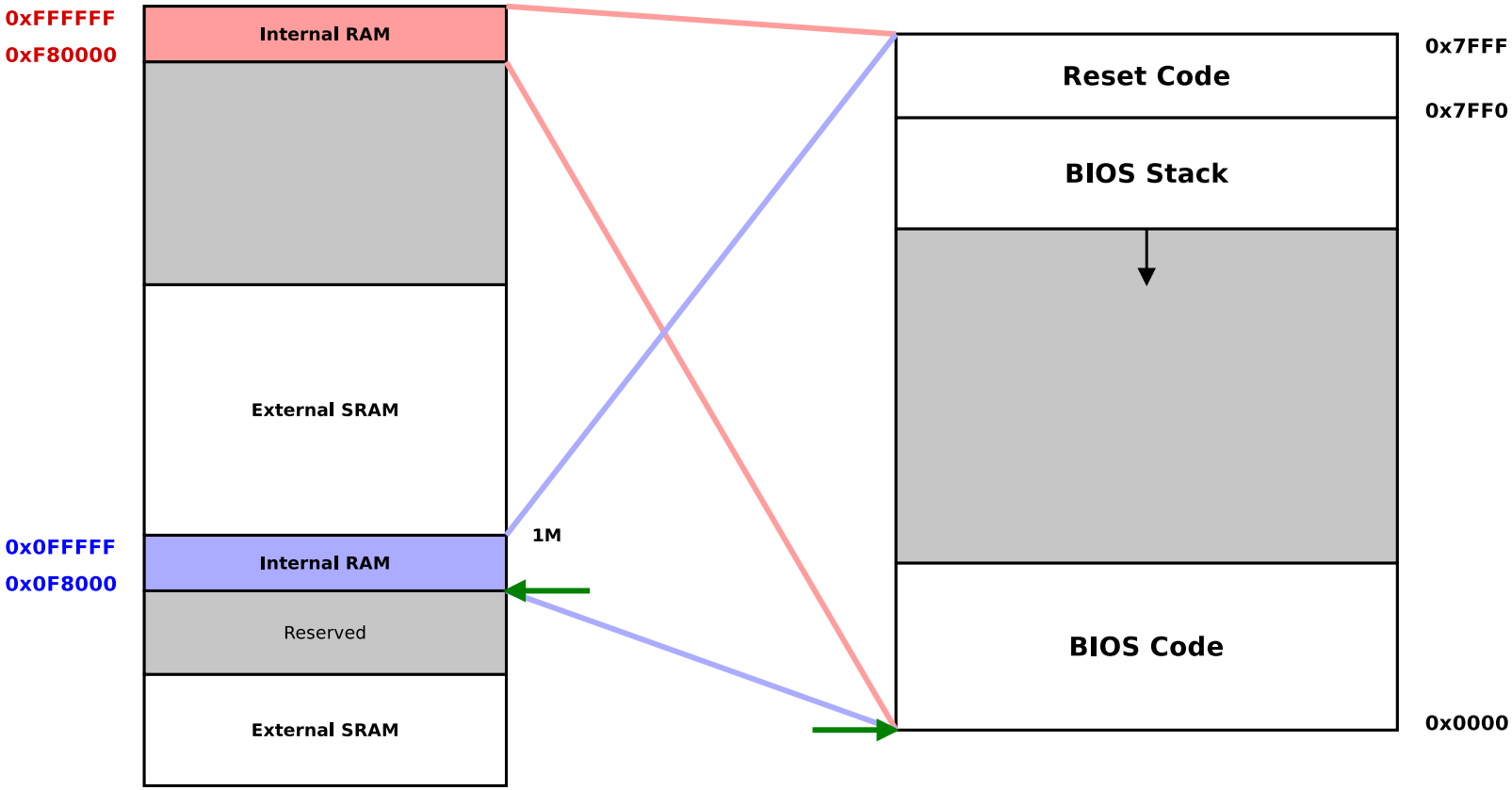
Reset


```
jmp 0xF000, 0x8000
```

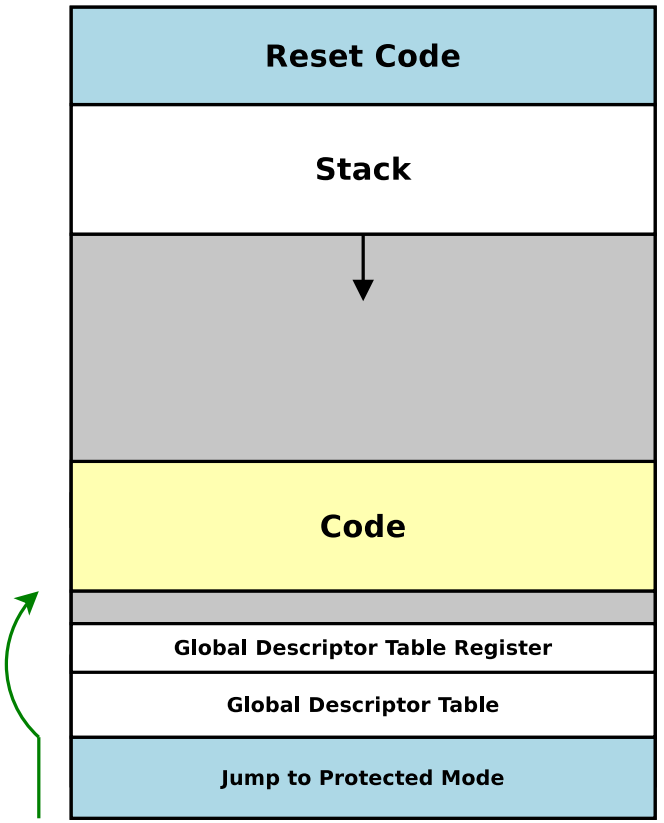


Reset


```
jmp 0xF000, 0x8000
```

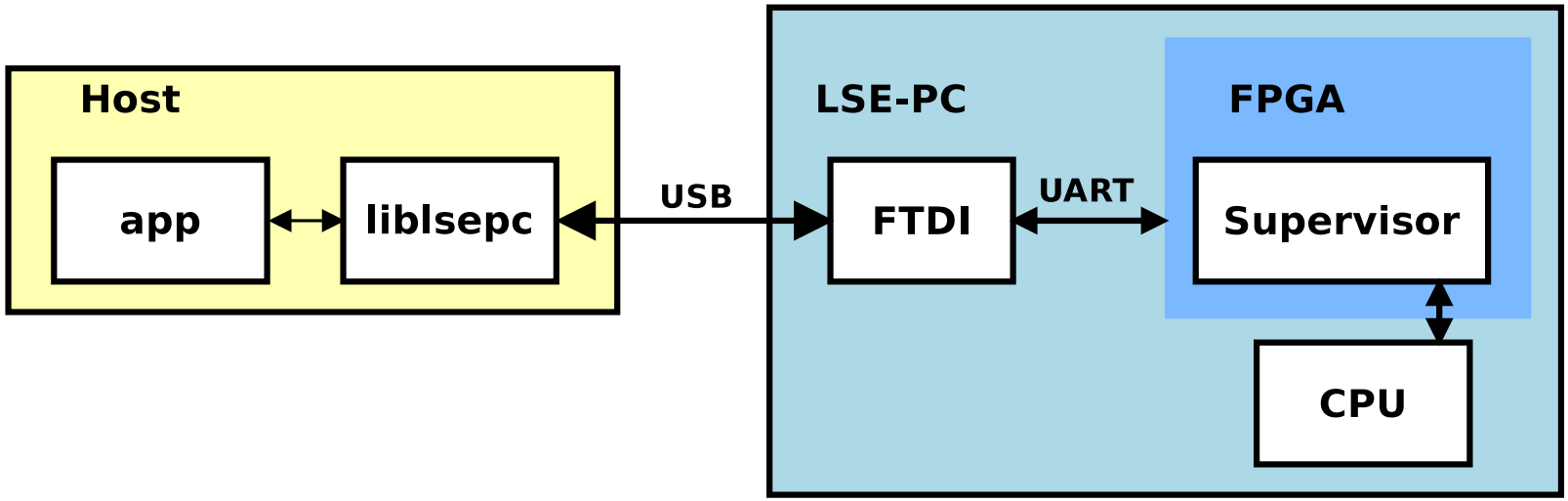


Protected Mode

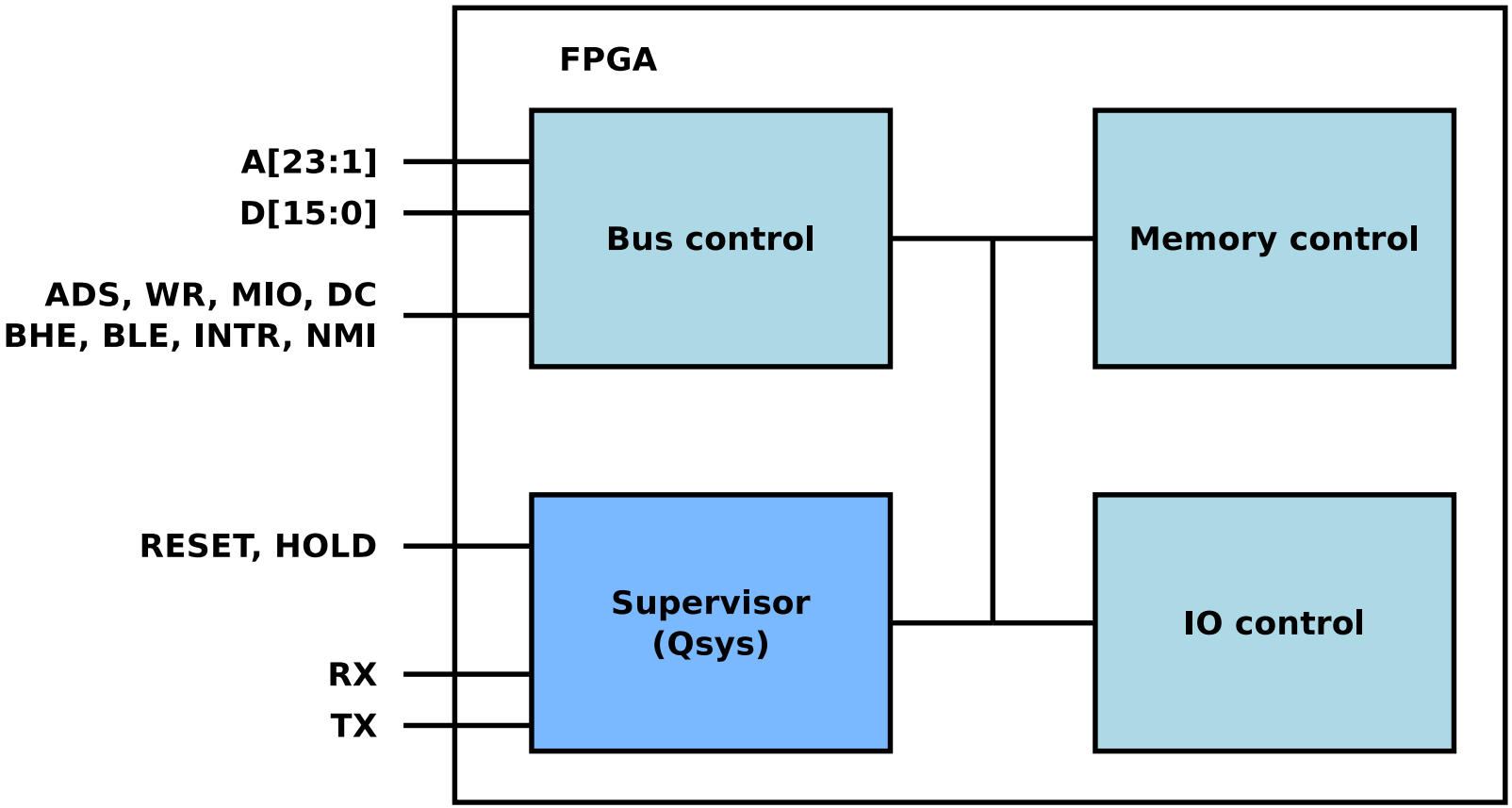



```
org 0x8000
startup:
    lgdt [gdtr]

    mov eax, cr0
    or eax, 1
    mov cr0, eax

    mov ax, 0x10
    mov ds, ax
    mov ss, ax

    ;; ljmp 0x08:0xF8400
    dw 0xEA66
    dd 0xF8400
    dw 0x08

align 16
gdt:    ...
gdtr:
    Limit dw gdtr - gdt - 1
    Base dd 0xF0000 + gdt
```

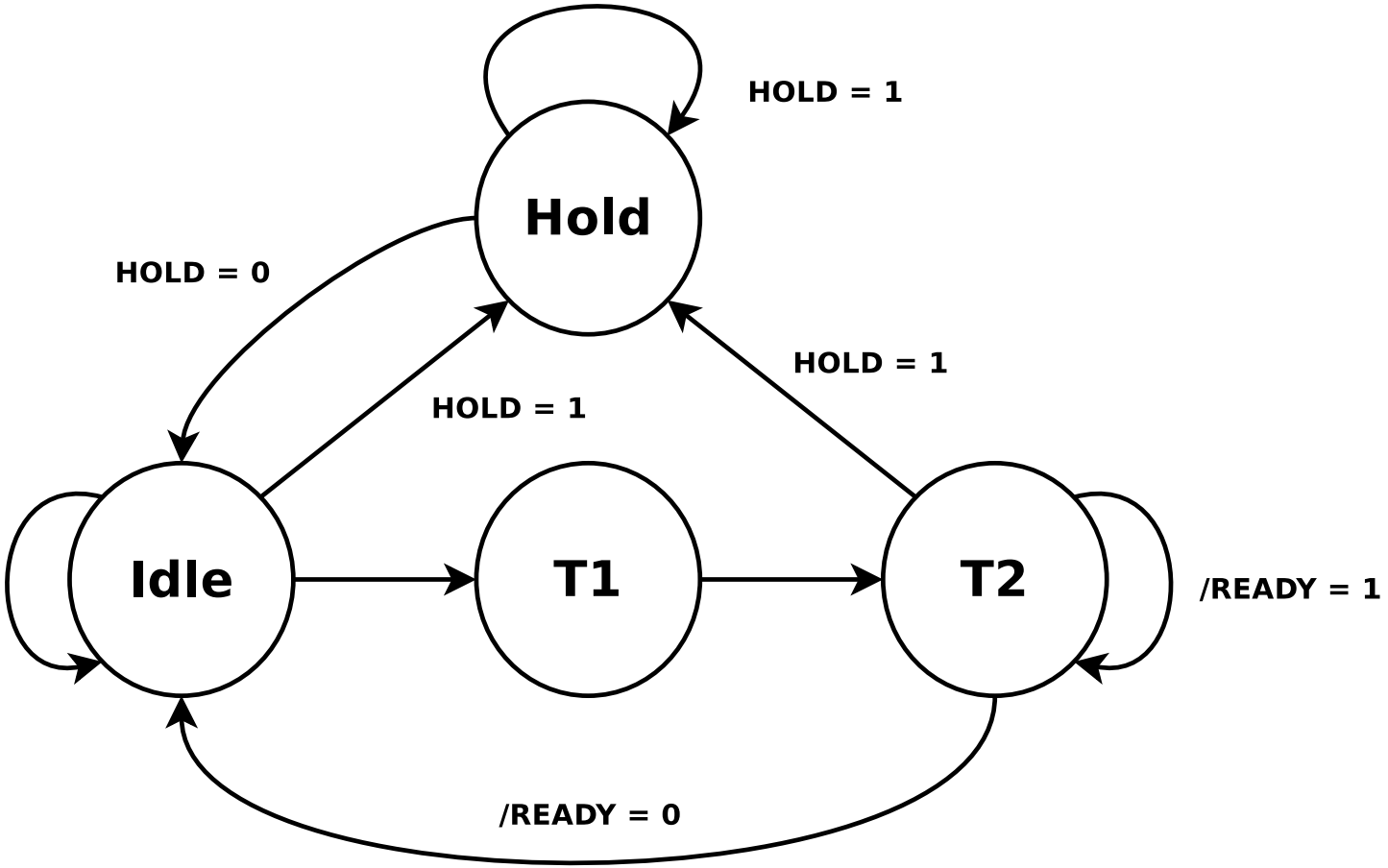
Application



Block Diagram



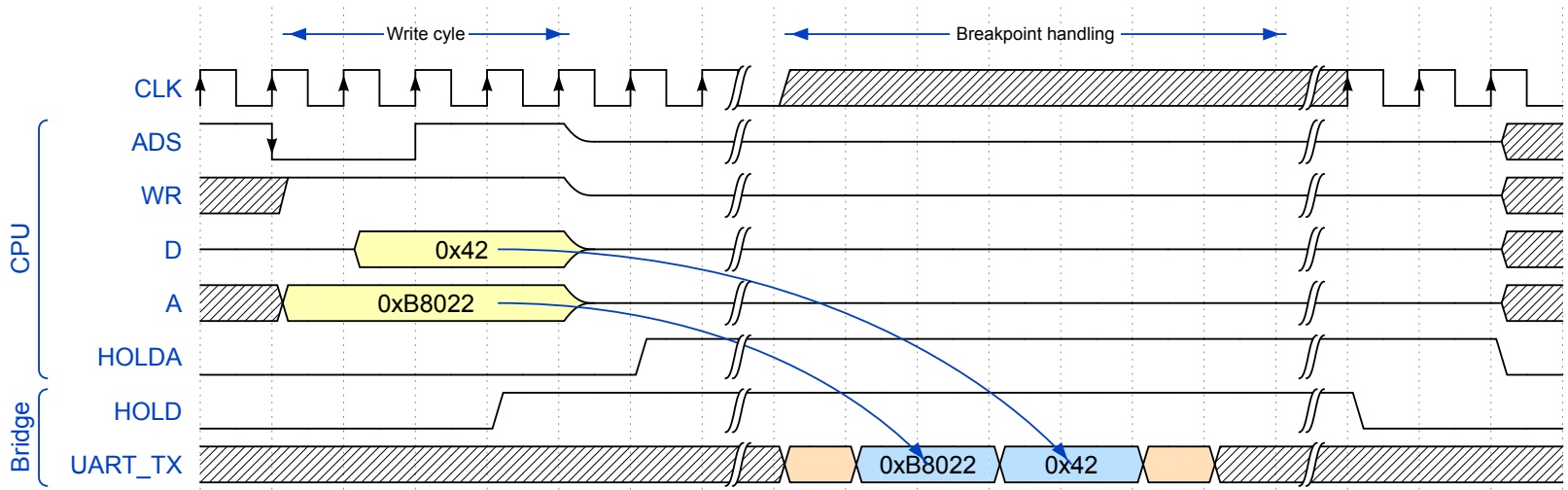
Hold State



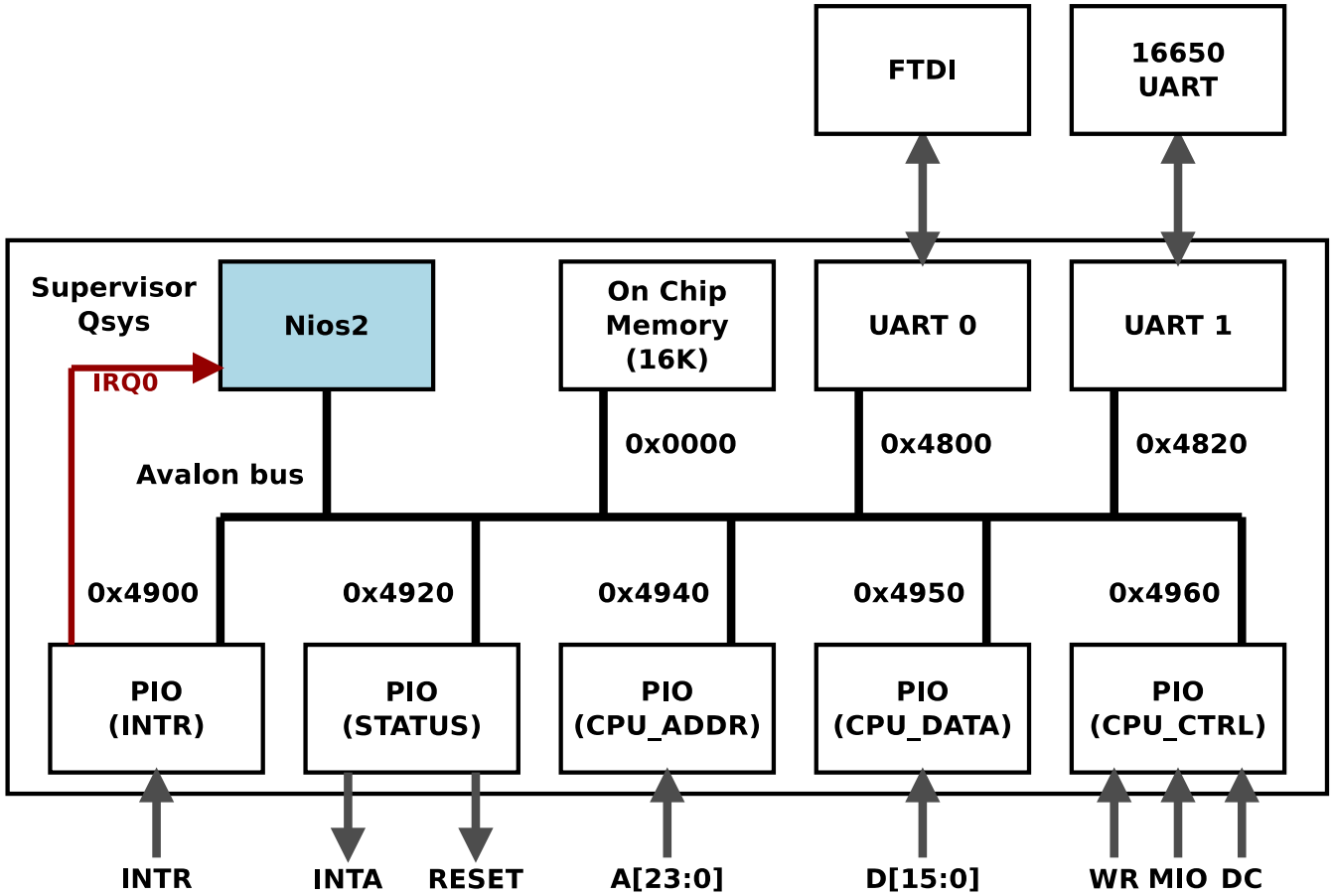
- *Hold*:
  - HOLDA $\leftarrow 1$
  - A, ADS, WR, DC, D, ... $\leftarrow$ Hi-Z

Breakpoint Handling

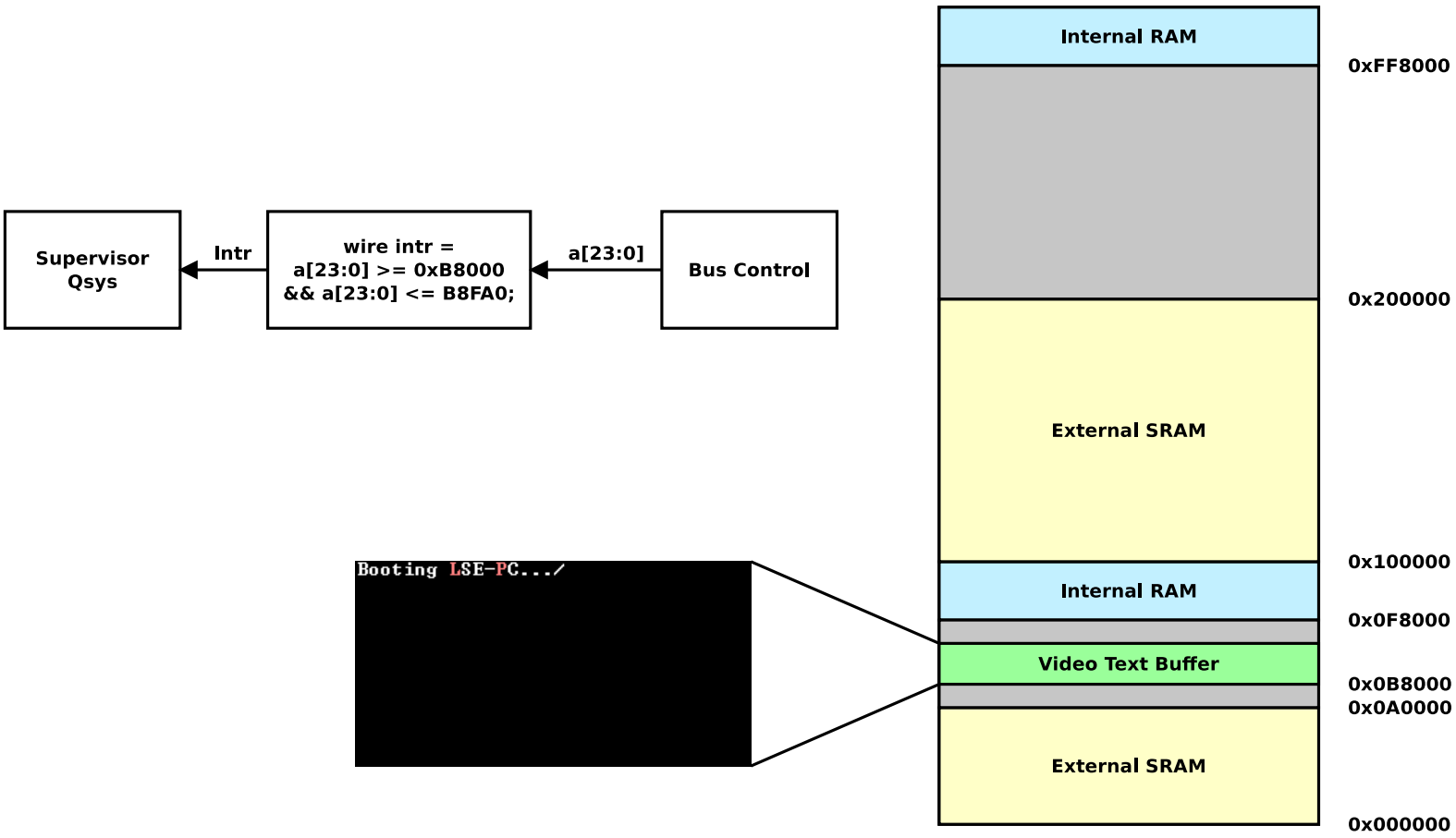

```
mov ax, 0xB800
mov gs, ax
mov al, 0x42
mov [gs:0x22], al
```



Supervisor Qsys



Emulated Framebuffer



Emulated Framebuffer

LSE-PC interfaces

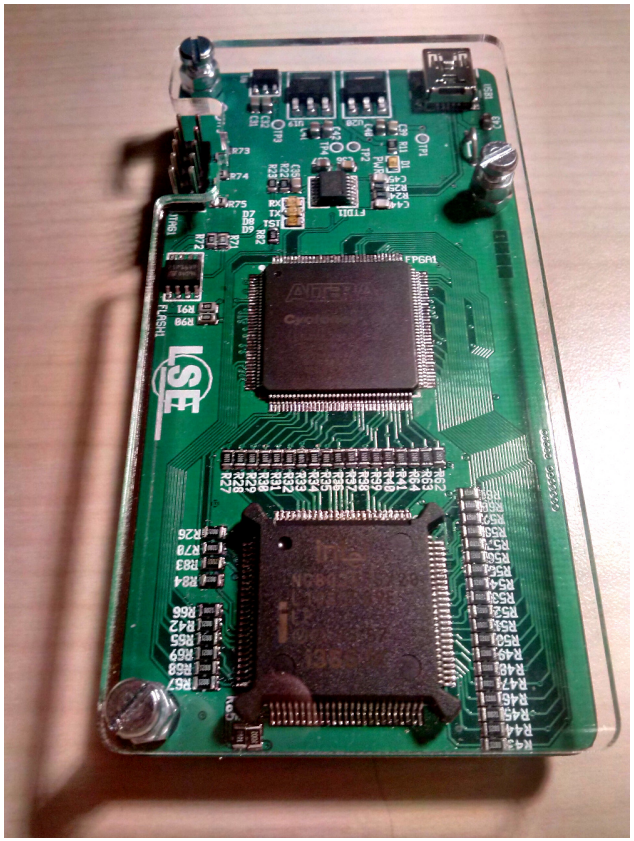
JTAG

```
$ jtagconfig -d
1) USB-Blaster [3-1.2]
  020F30DD   EP3C25/EP4CE22 (IR=10)
    Node 08186E00  ROM/RAM/Constant #0
    Node 19104600  Nios II #0
    Node 18206E00  Serial Flash loader #0
    Node 30006E00  SignalTap #0
    Design hash    D8426D4D2FFCB17E6612
```

USB

```
$ lsusb
Bus 003 Device 056: ID 0403:6015 Future Technology
Devices International, Ltd Bridge(I2C/SPI/UART/FIFO)
...
$ ls /dev/ttyUSB*
/dev/ttyUSB0
```

Q&A



- lse-pc.readthedocs.org
- #lse-pc@irc.rezosup.org
- Ptishell@irc.rezosup.org
- surply@lse.epita.fr
- @Ptishell