Open Source FPGA Toolchain

LSE Summer Week 2015

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What is a FPGA?

- Field Programmable Gate Array

Usage

- SDR (BladeRF, USRP)
- Pebble Time watch
- LSE-PC
- Prototypage

FPGA manufacturers

- Majors (80% market share): Altera, Xilinx
- Minors: Lattice, Blue Silicon, Microsemi,...

How to program a FPGA?

- Hardware Description Language (Verilog, VHDL)

Verilog example

```
module toplevel(input clock,
                input reset);

reg cnt;

always @ (posedge reset or posedge clock)
    if (reset)
        cnt <= 0;
    else
        cnt <= cnt + 1;
endmodule
```

Synthesis tools

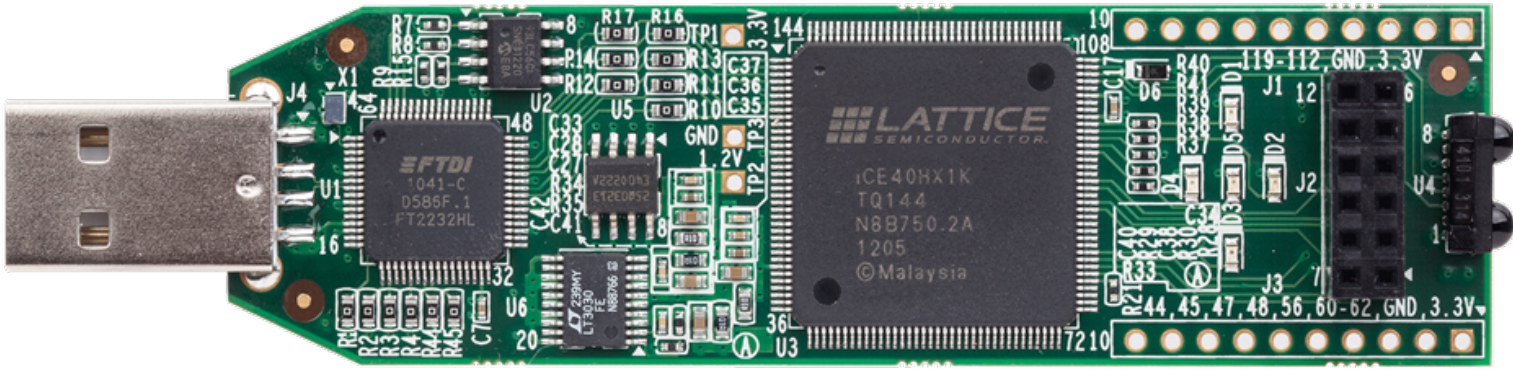
- Quartus by Altera
- Diamond (or Icecube 2) by Lattice

Why would we want an open source toolchain?

- Quartus $>$ 13.1 can't program (old) cyclones
- Linux support?
- Knowledge
- Why not?

iCE40

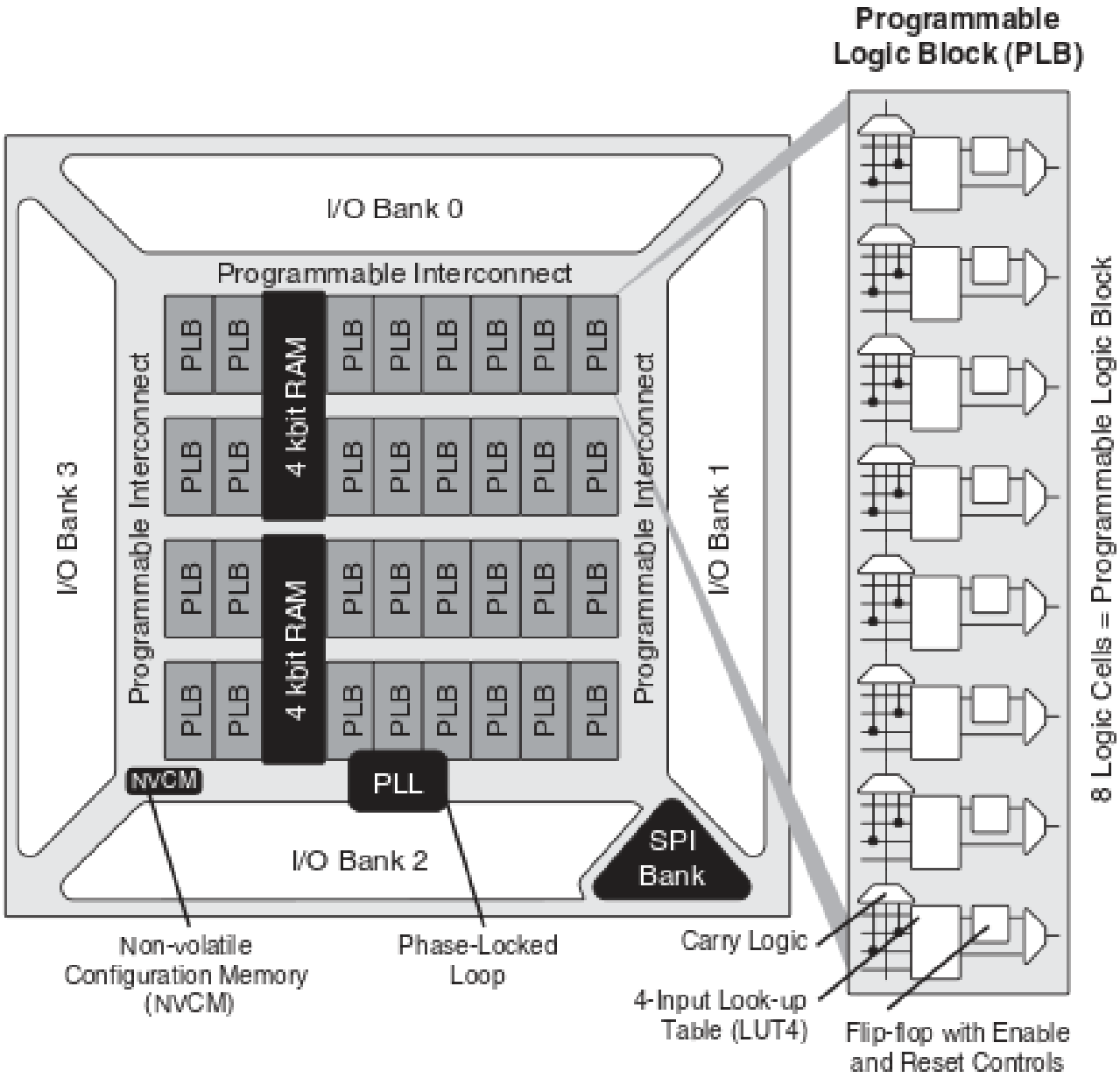
- Produced by Lattice semiconductor
- Low cost, low power FPGA
- Cheap boards and well documented
- Perfect platform to do some reverse engineering



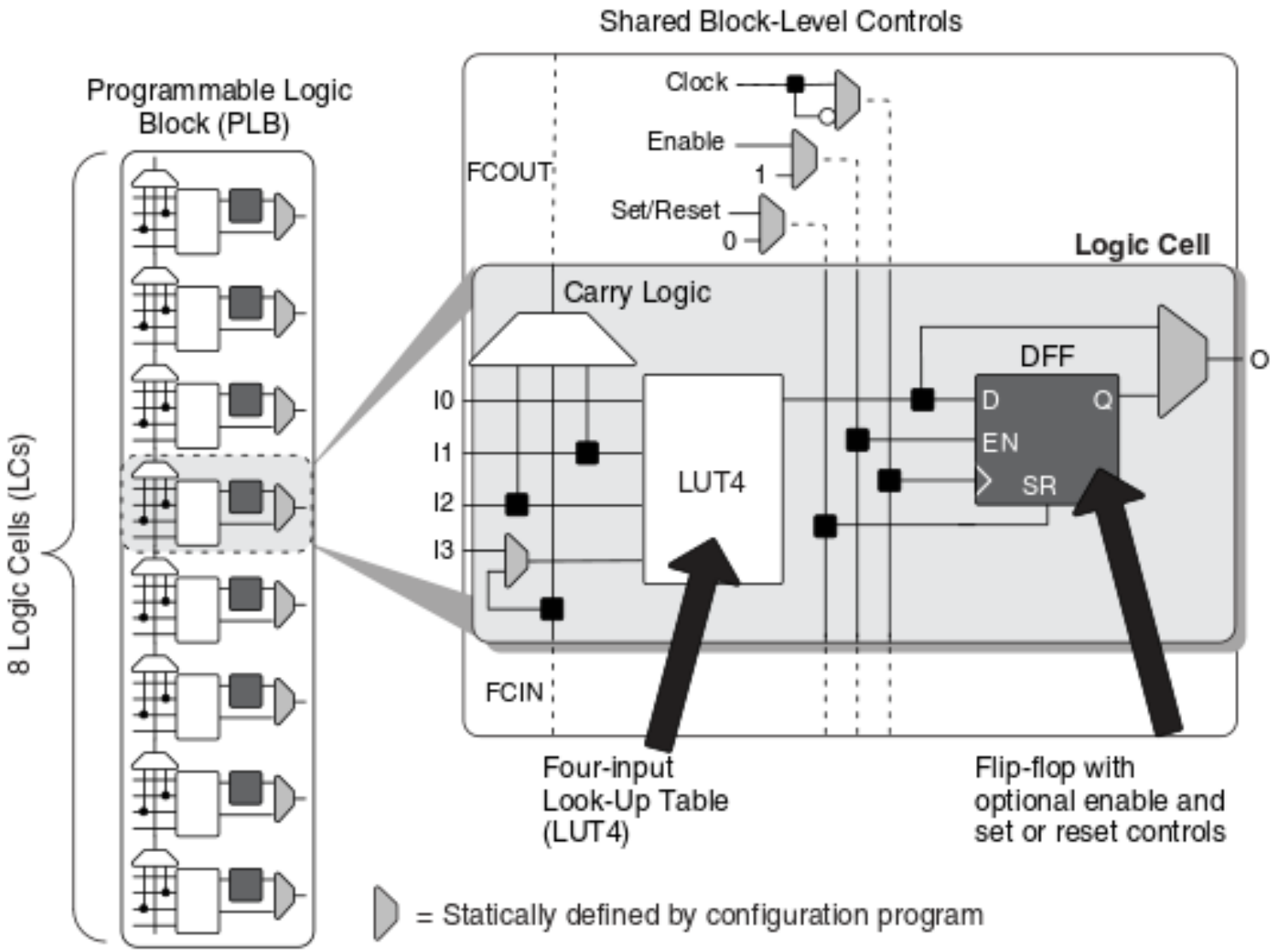
Project Icestorm

- iCE40 bitstream RE by Clifford Wolf and Mathias Lasser
- Aim to document iCE40 programming bits
- Many tools to pack, unpack, explain structures

iCE40 Structure



PLB Structure



Routing

	IO (1 17)	IO (2 17)	IO (3 17)	IO (4 17)	IO (5 17)	IO (6 17)	IO (7 17)	IO (8 17)	IO (9 17)	IO (10 17)	IO (11 17)	IO (12 17)	
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IntraPLB routing

- Local tracks
- Each PLB has 32 local tracks
- Organized in 4 groups of 8 wires each

InterPLB routing

	IO (1 17)	IO (2 17)	IO (3 17)	IO (4 17)	IO (5 17)	IO (6 17)	IO (7 17)	IO (8 17)	IO (9 17)	IO (10 17)	IO (11 17)	IO (12 17)	
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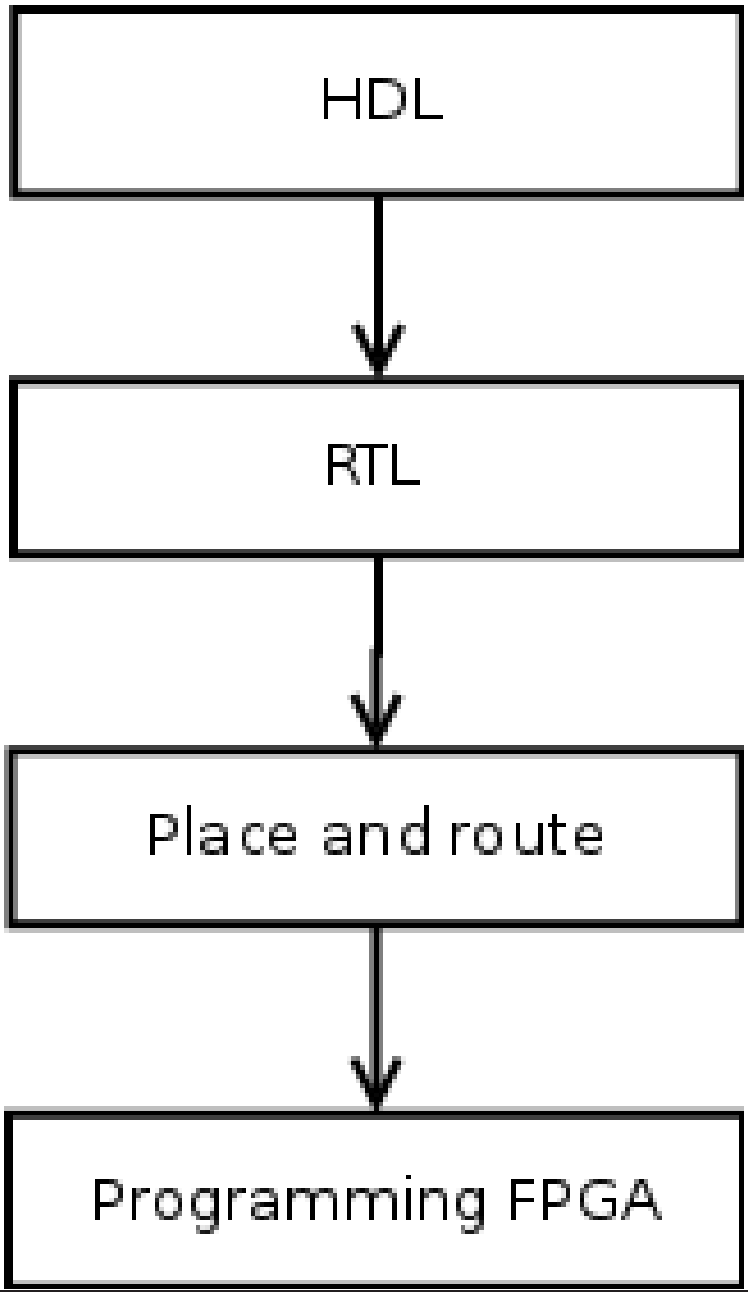
Programming process



Yosys

- Yosys Open Synthesis Suite
- Created by Clifford Wolf
- HDL to RTL synthesis tool

Yosys

Example

```
# read design
read_verilog mydesign.v

# generic synthesis
synth -top mytop

# write synthesized design
write_verilog synth.v
```

Arachne-pnr

- Place and route software aimed at iCE40LP/HX1K
- Written by Cotton Seed
- Takes RTL and constraints files (pin assignation)
- Output plain text cells configurations

constraints.pcf

```
set_io a 1
set_io b 10
set_io y 11
```

Icestorm

- Icepack: plain text to bitstream
- Iceunpack: bitstream to plain text
- IceProg: Program board

Example

and.v

```
module top (input a, b, output y);
    assign y = a & b;
endmodule
```

and.pcf

```
set_io a 1
set_io b 10
set_io y 11
```

Example


```
.io_tile 0 14
IOB_1 PINTYPE_0
IoCtrl IE_1
IoCtrl REN_0
buffer io_1/D_IN_0 span4_horz_28

.logic_tile 1 11
LC_2 0000000001010101 0000
buffer local_g1_4 lutff_2/in_3
buffer local_g3_1 lutff_2/in_0
buffer neigh_op_lft_4 local_g1_4
buffer sp4_r_v_b_41 local_g3_1
```

Conclusion

- This is still a proof of concept

Questions?

Questions?

Thanks!

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Links

- Yosys
- arachne-pnr
- icestorm