# Memory protection on AVR32

## LSE Summer Week 2014

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# AVR32 Architecture



- 32-bit RISC microprocessor
- Modified Harvard
- Up to 15 general-purpose 32-bit registers
- Instruction length : 16 bits
- Big-endian
- Fast interrupts and multiple interrupt priority levels
- Privileged and unprivileged modes

# AVR32 AP7



- Application Processors
- 221 DMIPS @ 150 MHz
- SIMD/DSP Instructions
- Instruction and Data caches
- Memory Management Unit
- Java hardware acceleration

# NGW100 Development Board



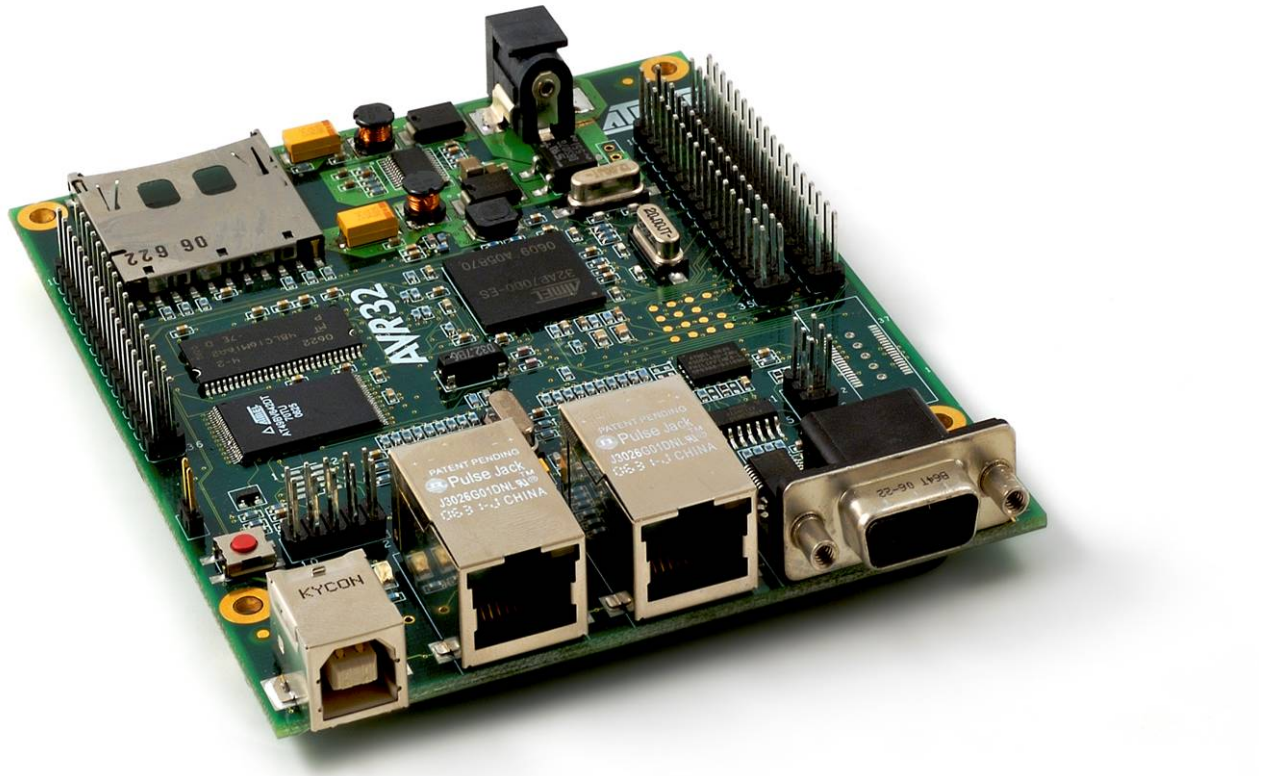


Figure: NGW100

# AVR32 UC3



- Flash Microcontrollers
- 91 DMIPS @ 66 MHz
- DSP Instructions
- Instruction and Data prefetch
- Memory Protection Unit
- Embedded Flash/RAM

# UC3 Development Board




Figure: EVK1100

# Memory Layout



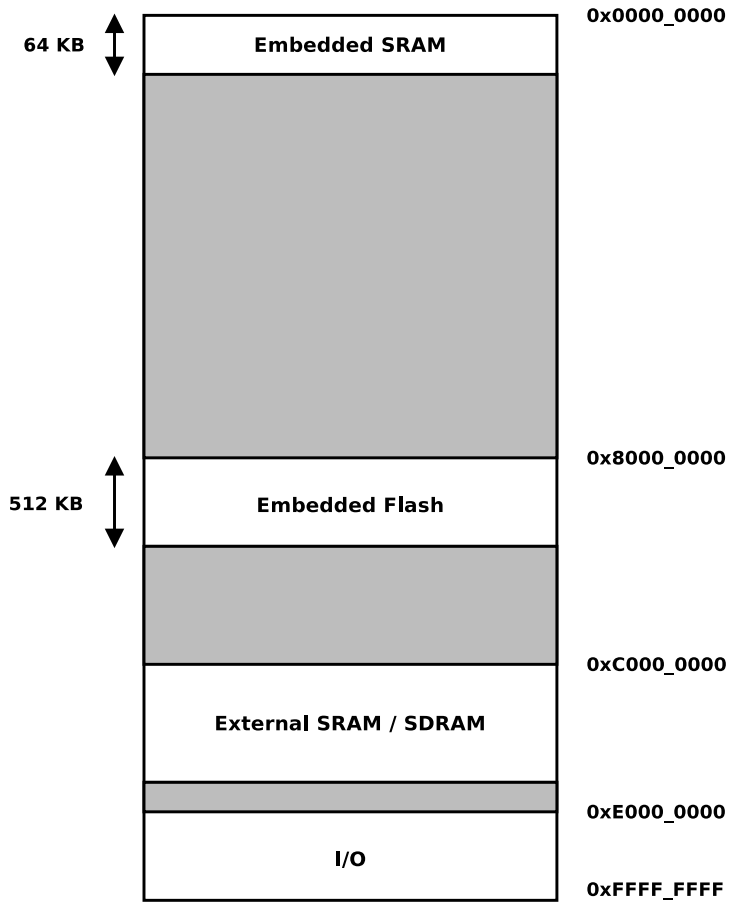


Figure: Memory Map (0x00000000 - 0xFFFFFFFF)

# Memory Layout



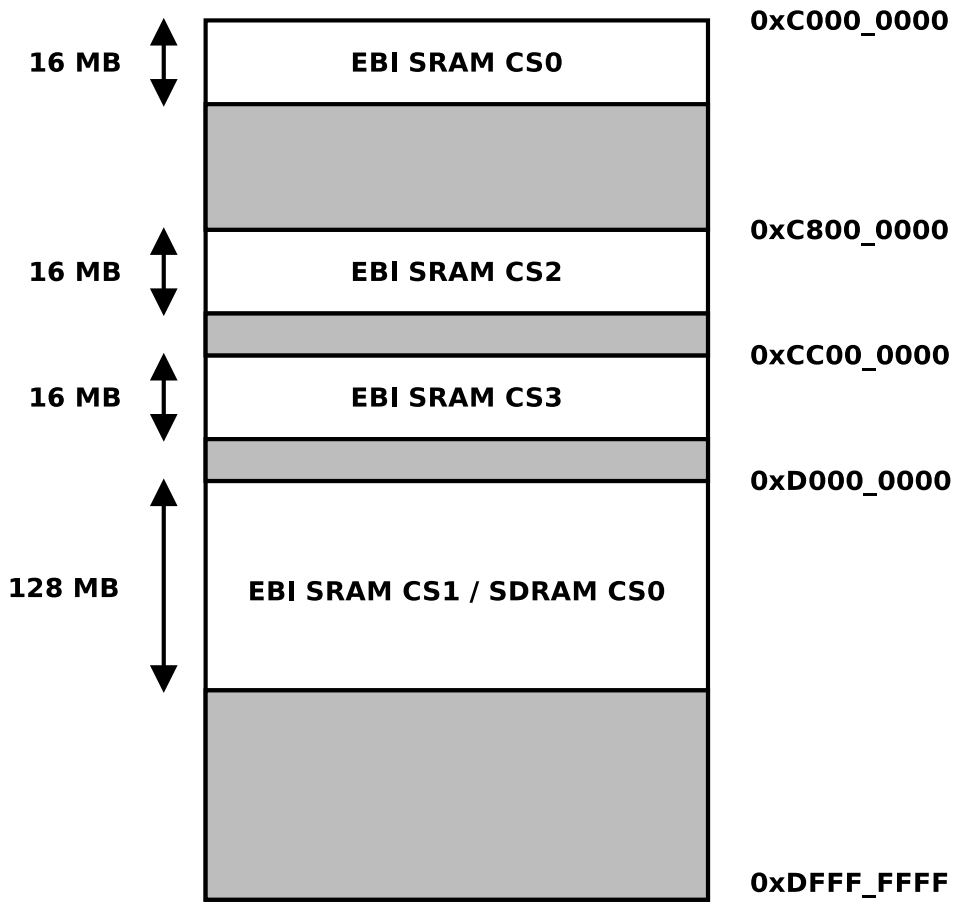


Figure: Memory Map (0xC0000000 - 0xDFFFFFFF)

# External Bus Interface



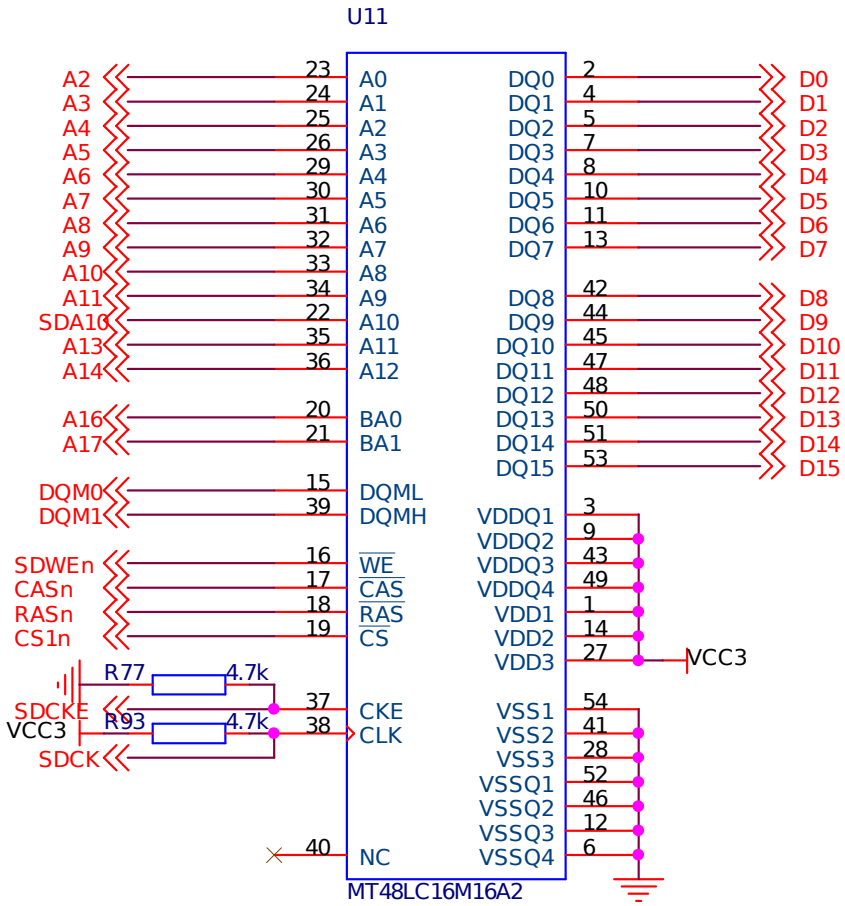


Figure: Synchronous DRAM 32MB - 4M x 16 x 4 banks

# External Bus Interface



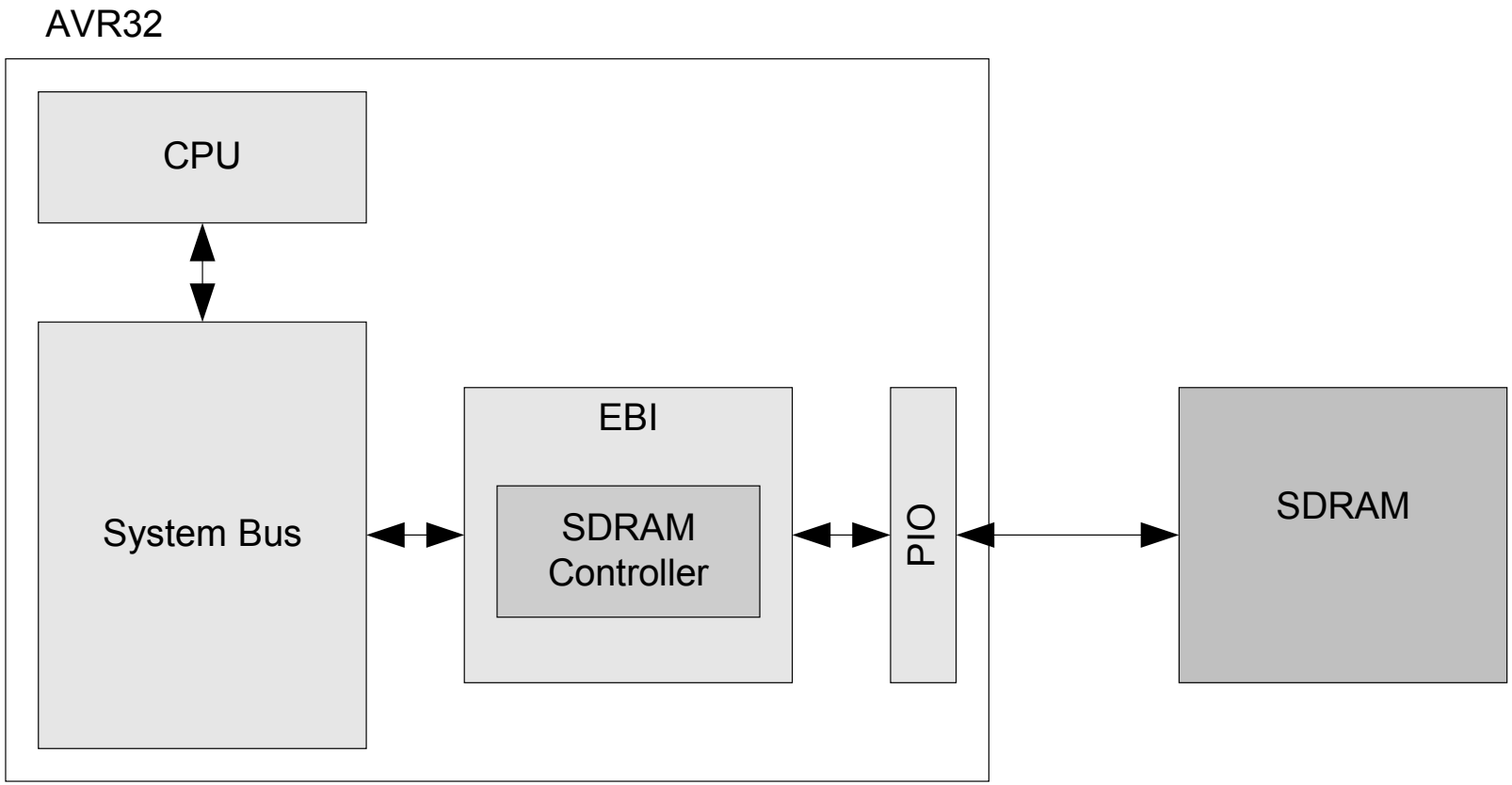


Figure: EBI Conceptual schematics

# External Bus Interface



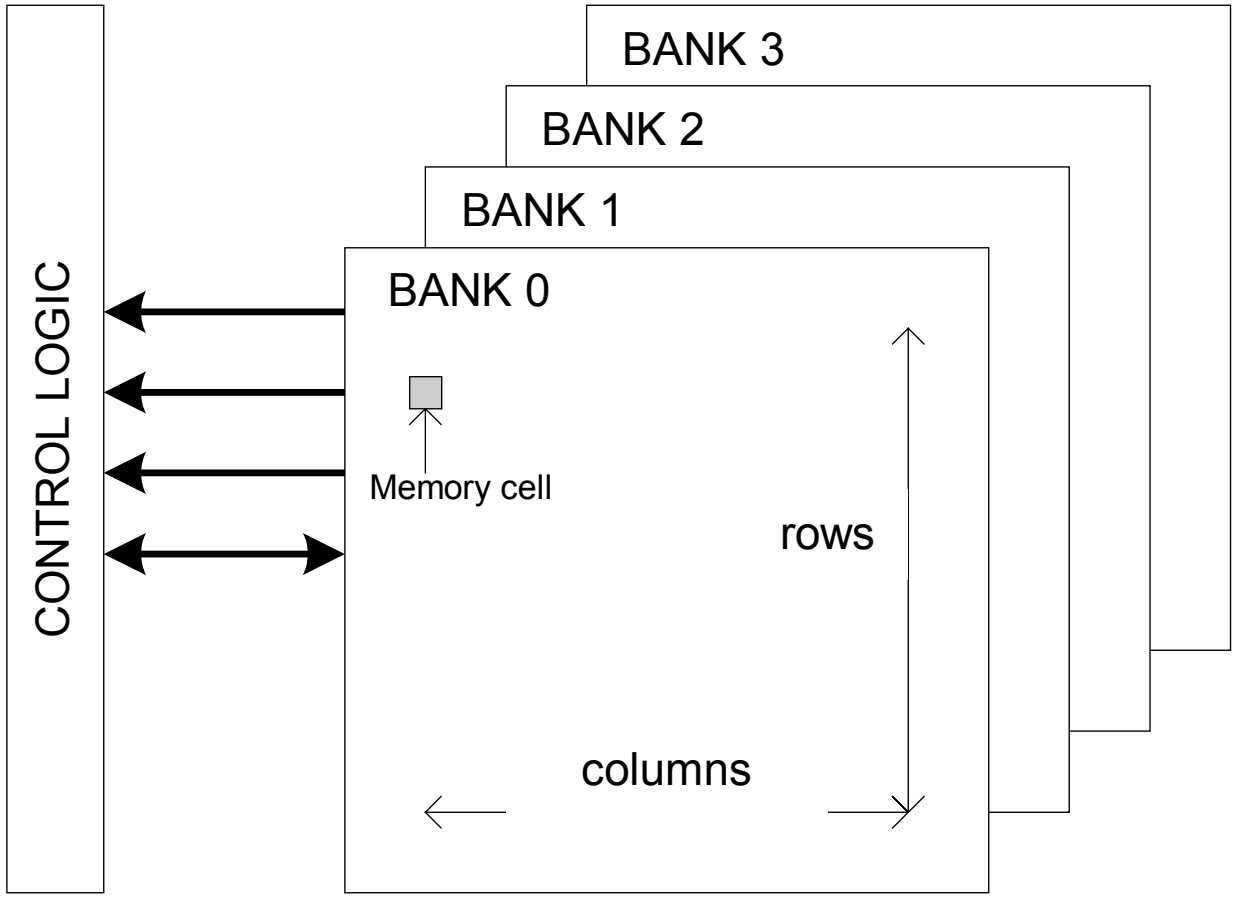


Figure: Generic SDRAM device

# External Bus Interface



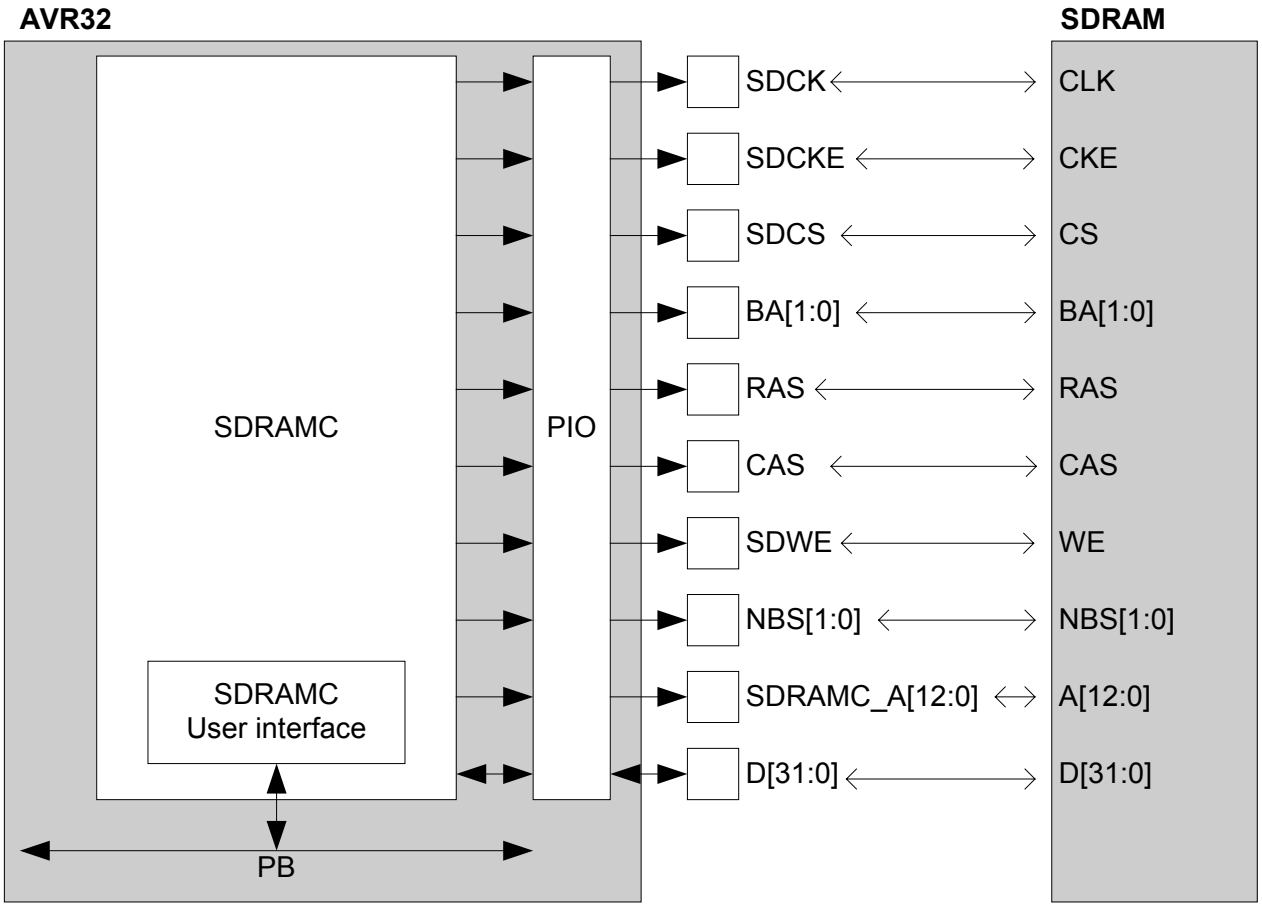


Figure: SDRAM Connection

# External Bus Interface



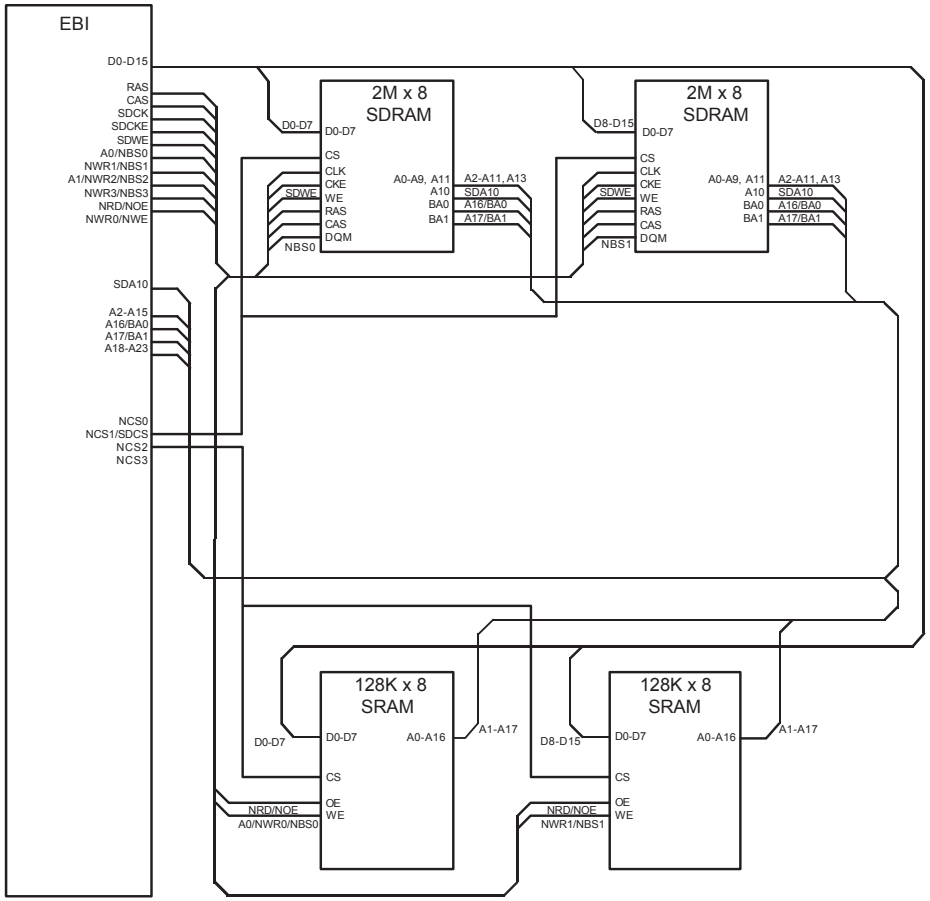


Figure: EBI Connections to Memory Devices

# Memory Protection Unit



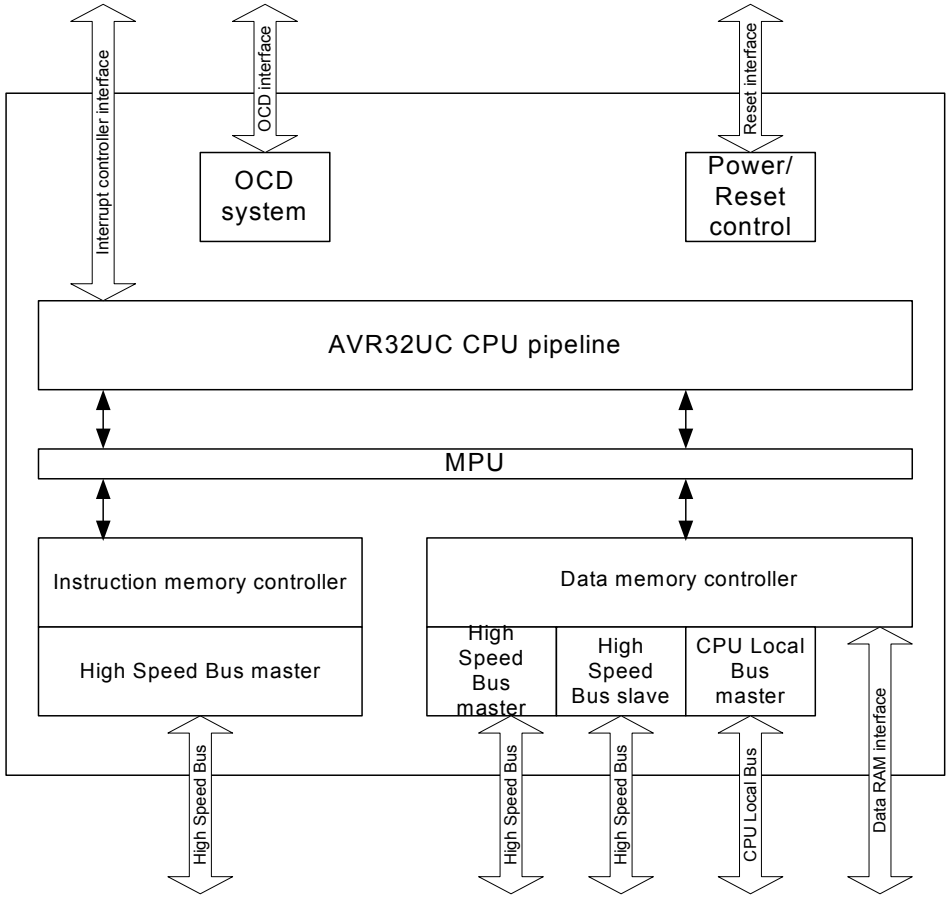


Figure: Overview of the AVR32UC CPU

# Memory Protection Unit



- Allows the user to divide the memory space into different protection regions.
- Each region is divided into 16 subregions, each of these subregions can have one of two possible sets of access permissions.

**AVR32 Architecture Document**

*This is a simpler alternative to a full MMU, while at the same time allowing memory protection.*

# MPU Exception Handling



- ITLB Protection Violation
- DTLB Protection Violation
- ITLB Miss Violation
- DTLB Miss Violation
- TLB Multiple Hit Violation

# Memory Protection Unit



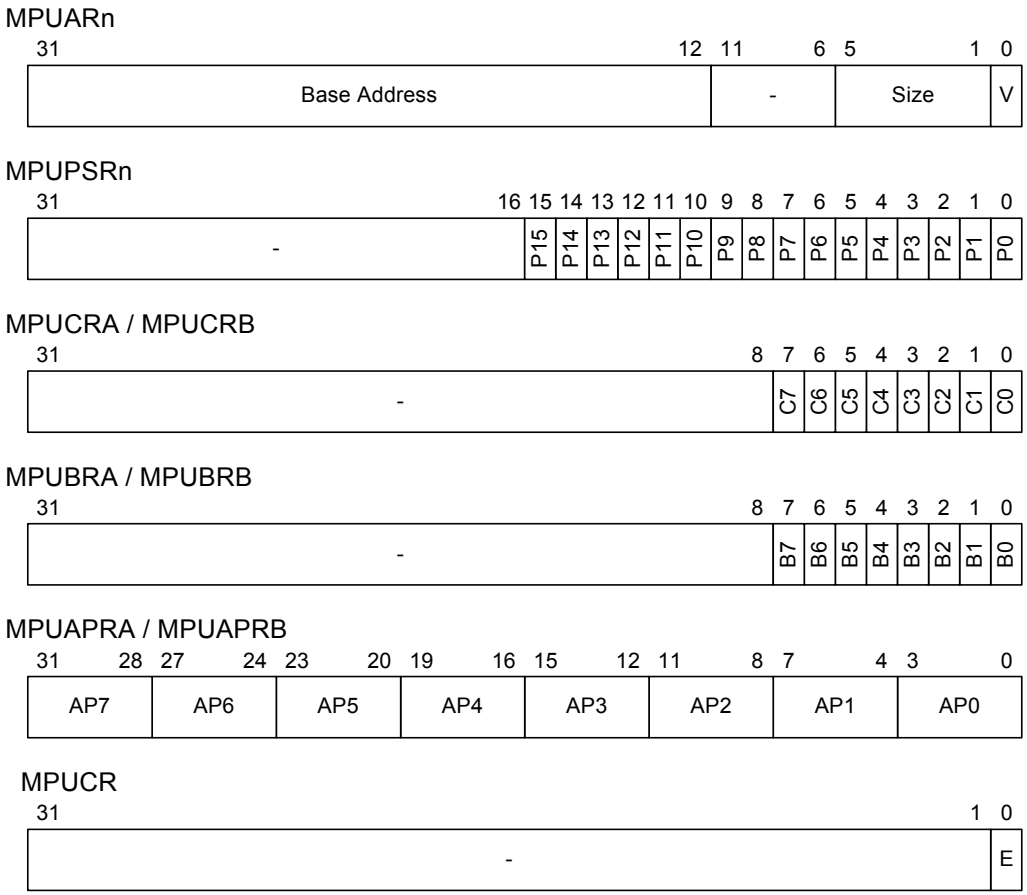


Figure: MPU Registers

# System Registers



```
__asm__ volatile ("mfsr %0, %1"
                  : "=r" (res)
                  : "i" (addr));

__asm__ volatile ("mtsr %0, %1"
                  :
                  : "i" (addr),
                    "r" (value));
```

# Memory Protection



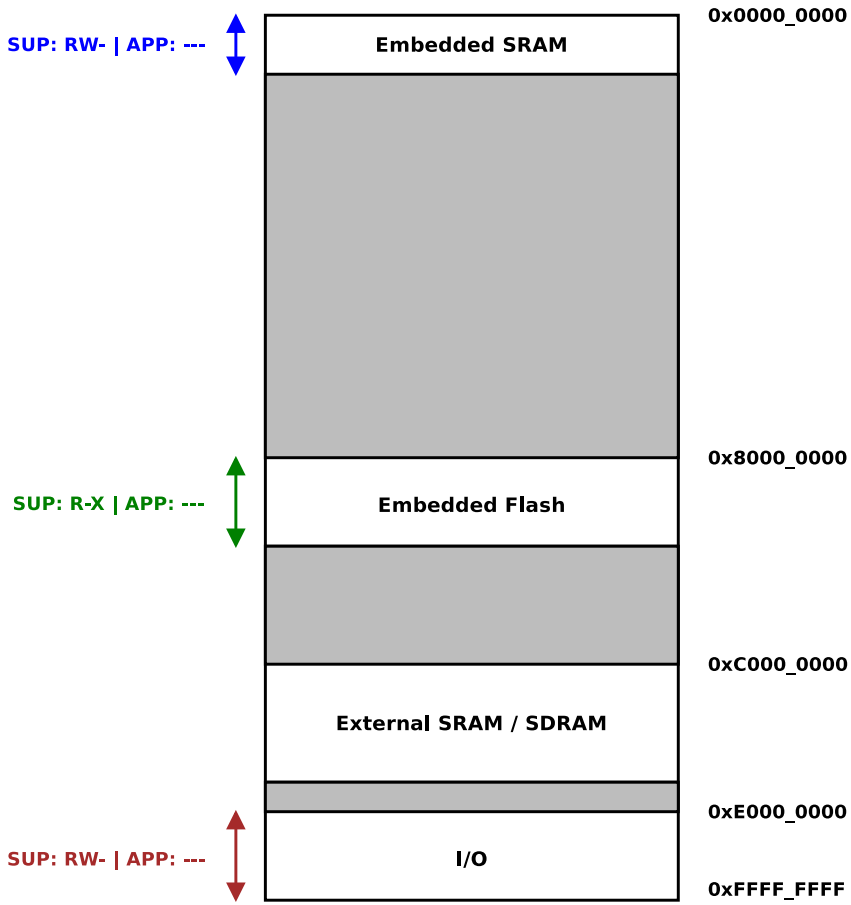


Figure: Basic MPU configuration

# Memory Protection



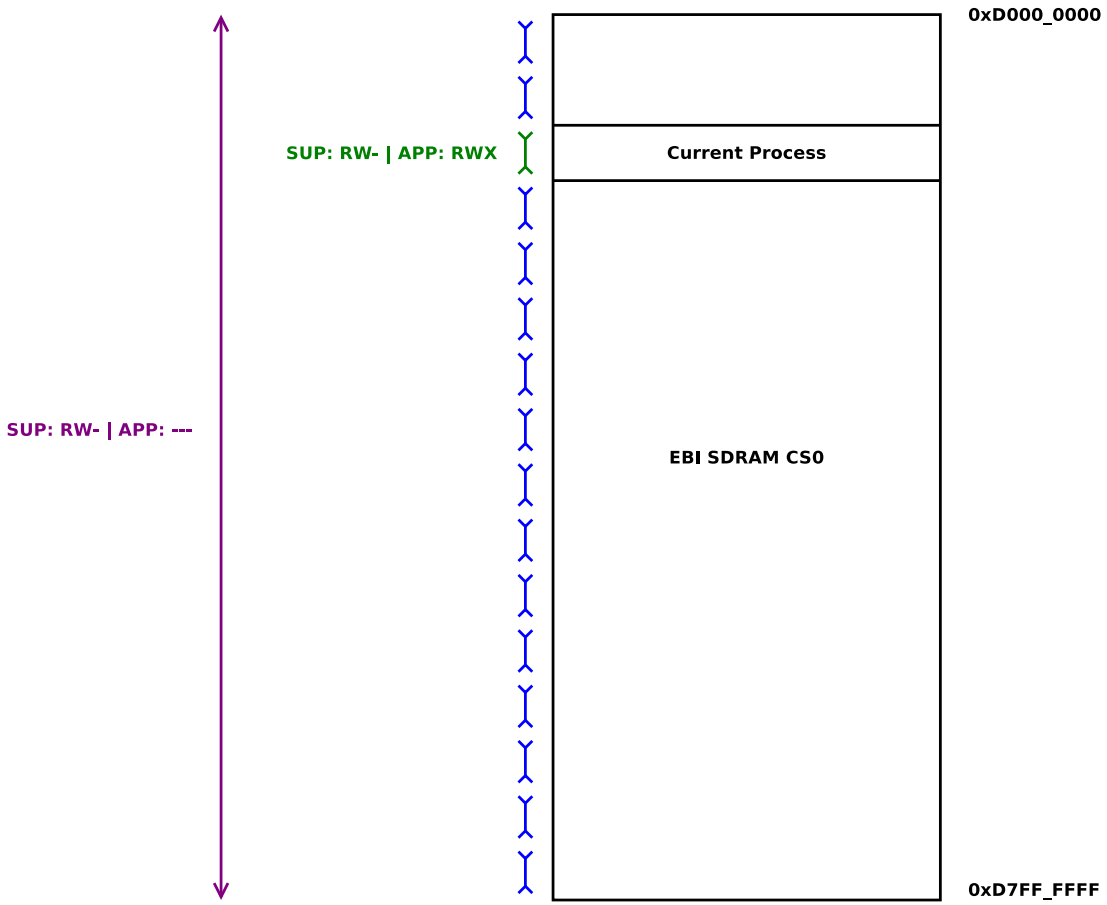


Figure: Application MPU configuration I

# Memory Protection



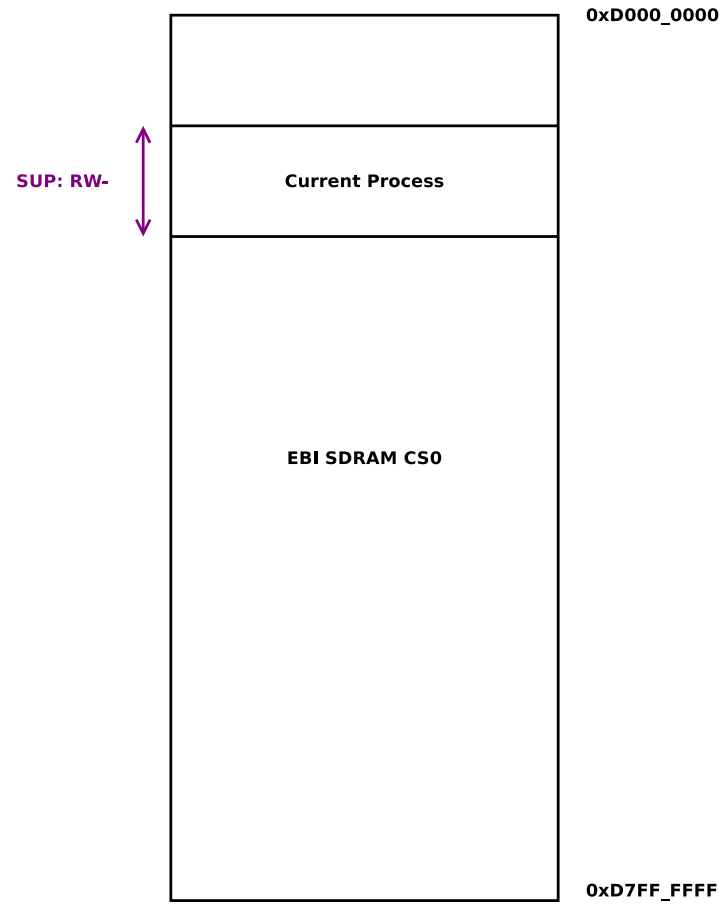


Figure: Application MPU configuration II

# Memory Protection



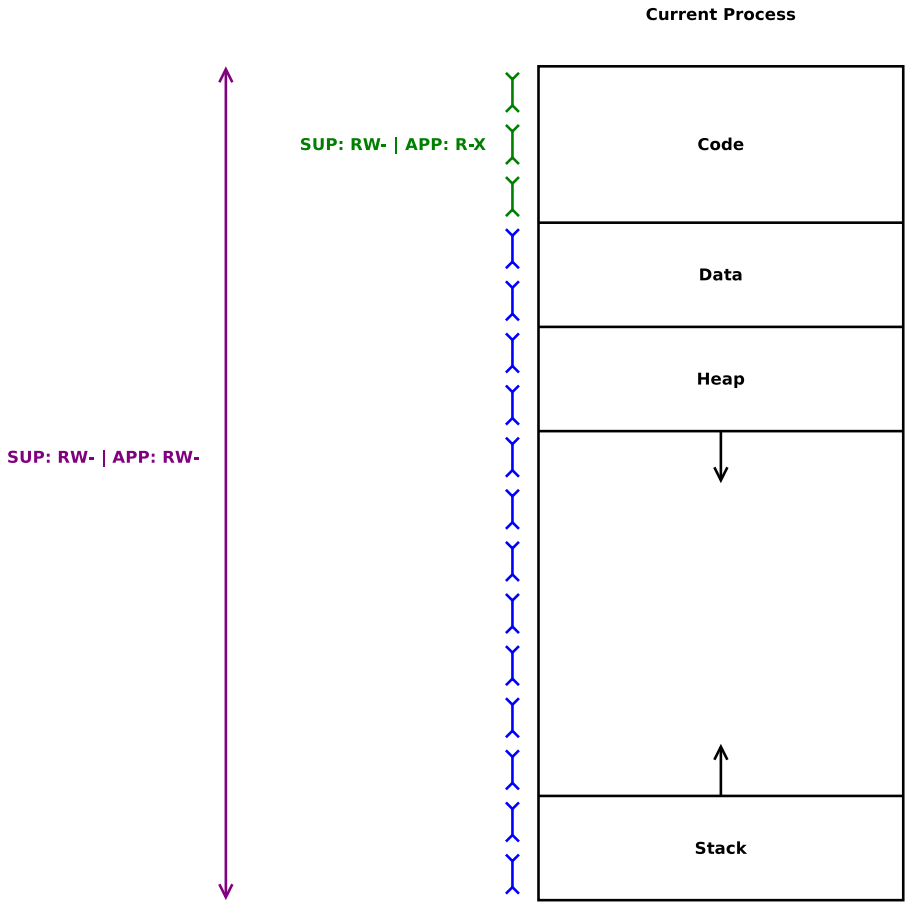


Figure: Application address space

# Memory Protection



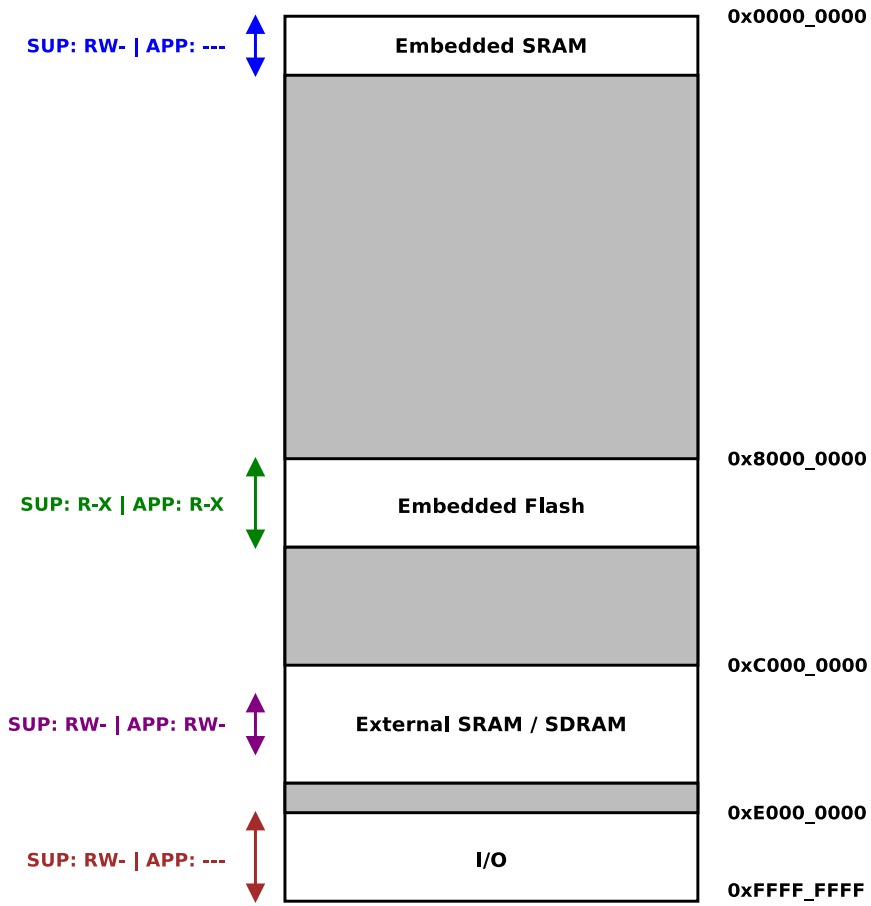


Figure: Builtin MPU Configuration

# Conclusion



- Not an alternative to a full MMU
  - Limited number of regions
  - Fixed size regions
- FreeRTOS-MPU
  - `vTaskAllocateMPURegions()`
  - `portSWITCH_TO_USER_MODE()`
  - `xTaskCreate()` -> `xTaskCreateRestricted()`

# Contact



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